Refine Search

Search Results -

Terms	Documents
compar$3 near5 (trigger adj1 condition)near10 bus	1

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DATE: Thursday, May 20, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L1	compar$3 near5 (trigger adj1 condition)near10 bus	1	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
compar$3 near5 (trigger adj1 condition)near10 bus	1

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Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L1	compar$3 near5 (trigger adj1 condition)near10 bus	1	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
compar$3 same (trigger adj1 condition)same bus	19

Database:
US Pre-Grant Publication Full-Text Database
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Search: L2

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Recall Text | Clear | Interrupt

Search History

DATE: Thursday, May 20, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L2	compar$3 same (trigger adj1 condition)same bus	19	L2
L1	compar$3 near5 (trigger adj1 condition)near10 bus	1	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
compar$3 same (trigger adj1 condition)same bus	19

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
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Search: L3

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Thursday, May 20, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	compar$3 same (trigger adj1 condition)same bus	19	L3
L2	compar$3 same (trigger adj1 condition)same bus	19	L2
L1	compar$3 near5 (trigger adj1 condition)near10 bus	1	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Freeform Search

Database: US Pre-Grant Publication Full-Text Database
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US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Term: compar$3 same (trigger adj1 condition)same bus

Display: 10 **Documents in Display Format:** - **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search Clear Interrupt

Search History

DATE: Thursday, May 20, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	compar$3 same (trigger adj1 condition)same bus	19	L3
L2	compar$3 same (trigger adj1 condition)same bus	19	L2
L1	compar$3 near5 (trigger adj1 condition)near10 bus	1	L1

END OF SEARCH HISTORY

Freeform Search

Database:
- US Pre-Grant Publication Full-Text Database
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Term: (5142673| 5210862| 5313618| 5325368| 5329471| 5355369| 5371551| 5375228| 5463760| 5488688| 5513338| 5530804| 5535412| 5539901| 5544311|

Display: 10 **Documents in Display Format:** - **Starting with Number** 1

Generate: ○ Hit List ◉ Hit Count ○ Side by Side ○ Image

Search | Clear | Interrupt

Search History

DATE: Thursday, May 20, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,USOC; PLUR=YES; OP=OR		
L5	(5142673| 5210862| 5313618| 5325368| 5329471| 5355369| 5371551| 5375228| 5463760| 5488688| 5513338| 5530804| 5535412| 5539901| 5544311| 5546566| 5560036| 5561761| 5566303| 5590354| 5610826| 5621651| 5623673| 5631910| 5640542| 5671172| 5729678| 5812830| 5908392| 5960457| 5999163| 6026503)! [pn]	32	L5
L4	6618775.pn.	1	L4
L3	compar$3 same (trigger adj1 condition)same bus	19	L3
L2	compar$3 same (trigger adj1 condition)same bus	19	L2
L1	compar$3 near5 (trigger adj1 condition)near10 bus	1	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and trigger$3.clm.	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
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EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Thursday, May 20, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
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L2	L1 and trigger.clm.	0	L2
L1	6609211.pn. or 6438697.pn. or 6233691.pn. or 6029249.pn.	4	L1

END OF SEARCH HISTORY

6 Claims, 4 Drawing figures

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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Terms	Documents
(5142673| 5210862| 5313618| 5325368| 5329471| 5355369| 5371551| 5375228| 5463760| 5488688| 5513338| 5530804| 5535412| 5539901| 5544311| 5546566| 5560036| 5561761| 5566303| 5590354| 5610826| 5621651| 5623673| 5631910| 5640542| 5671172| 5729678| 5812830| 5908392| 5960457| 5999163| 6026503)![pn]	32

Display Format: TI Change Format

Previous Page Next Page Go to Doc#

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First Hit Fwd Refs

End of Result Set

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L1: Entry 1 of 1 File: USPT Sep 9, 2003

DOCUMENT-IDENTIFIER: US 6618775 B1
TITLE: DSP bus monitoring apparatus and method

Abstract Text (1):
A bus monitor is provided as a tool for developing, debugging and testing a system having an embedded processor. The bus monitor resides within the same chip or module as the processor, which allows connection to internal processor buses not accessible from external contacts. The monitor uses a separate circular buffer to continuously store, in real-time, data traces from each of one or more internal processor buses. Upon the occurrence of a trigger condition, storage stops and a trace is preserved. Trigger conditions can depend on events occurring on multiple buses and are downloaded via an interface from an external device. Data traces are uploaded via the interface to an external device for evaluation of processor operation.

Brief Summary Text (13):
A bus monitor is co-located with a processor on a chip or within a module. The bus monitor includes an interface, a bus watching circuit and a memory. The interface provides a connection between the external contacts of the chip or module package and the bus monitor. The interface has an input which allows trigger conditions to be downloaded from an external device to the bus monitor. The interface also has an output which allows a captured trace of bus states to be uploaded to an external device. The bus watching circuit monitors the data on at least one of the processor buses, producing a trigger output when a triggering event matches the downloaded trigger condition. The memory stores data from at least one of the processor buses in response to the bus watching circuit trigger output, creating a trace of states occurring on a bus. The memory also reads trace data from its storage to the interface output.

Brief Summary Text (14):
Another aspect of the current invention is a method of monitoring processor bus states occurring on at least one of a plurality of internal processor buses. The method involves downloading a trigger condition from an external device to the bus monitor. The downloaded trigger condition is compared with events occurring on monitored buses. In response to a comparison match, a trace of bus data is retained in storage. This trace data is then uploaded to an external device for analysis.

Drawing Description Text (15):
FIG. 14, comprising FIGS. 14A-14M is a timing diagram illustrating the downloading of trigger point data through the external interface; and

Detailed Description Text (4):
FIGS. 3A-3B show a block diagram of the DSP of FIGS. 1A-1B incorporating a bus monitor according to the present invention. FIG. 4 shows a block diagram of the DSP of FIG. 2 incorporating a bus monitor according to the present invention. Referring to FIG. 3, the bus monitor 300 includes bus watching circuitry 310, a circular buffer 330, and an external interface 350. The bus watching circuitry 310 determines the occurrence of a triggering event on one or more processor buses. The

circular buffer 330 acts as the memory which stores bus data as a function of a triggering event. The external interface 350 allows a trigger condition to be downloaded to the bus monitor from an external device, such as a PC, and allows bus trace data to be uploaded from the bus monitor to an external device.

Detailed Description Text (5):
In one case, the bus monitor comprises a bus watching circuit which monitors conditions occurring on a single processor bus to trigger a circular buffer which stores data from a single processor bus. FIG. 3 illustrate this particular example where the bus watching circuitry 310 monitors conditions occurring on the DRAB bus 150 to trigger a trace of events occurring on the DRDB bus 160. The triggering event can, for example, occur when a value on a single bus is greater than, less than, or equal to a given value.

Detailed Description Text (6):
The bus monitor can be more sophisticated than watching a single bus to trigger data capture from a single bus. The bus watching circuit can monitor multiple buses and generate multiple triggers for the capture of data from multiple buses. For example, FIG. 5 illustrate a bus monitor 500 where the bus watching circuit 510 monitors six different DSP buses 110-160 and generates triggers 522, 524, 526 to three different circular buffers 532, 534, 536. These circular buffers capture data traces from three different DSP buses 140, 150, 160. If the bus watching circuitry is used to monitor multiple buses, the trigger event can be more complex than the example described above with respect to FIG. 3. For example, the triggering event can be a corresponding occurrence of an even value on an address bus and a specific operation code on an instruction bus.

Detailed Description Text (8):
FIG. 6 shows a detailed block diagram of a preferred embodiment of the bus monitor. The bus watching circuitry includes multiple bus matching functions and event matching functions to generate multiple circular buffer triggers. Each bus match circuit monitors a bus to determine the occurrence of a particular bus event, generating a "match" signal in response. A particular processor bus may be connected to zero, one or multiple bus match circuits. For example, FIG. 6 illustrates six processor buses A-F. Bus A 602 is monitored by the bus match 1 circuit 622 which generates the MATCH 1 signal 632. Bus B 604 is monitored by the bus match 2 circuit 624 which generates the MATCH 2 signal 634. Bus C 606 is unmonitored. Bus D 608 is monitored by both the bus match 3626 and bus match 4628 circuits which generate the MATCH 3636 and MATCH 4638 signals, respectively. Buses E 610 and F 612 are also unmonitored.

Detailed Description Text (9):
Multiple event match circuits are each connected to the match signals which are output from the bus match circuits. Each event match circuit responds to a particular combination of these match signals to generate a trigger signal to a particular circular buffer. Referring again to FIG. 6, match signals MATCH 1632, MATCH 2634, MATCH 3636 and MATCH 4638 are routed to each of three event match circuits, event match 1642, event match 2644, and event match 3646. Each of these event match circuits, in response to its particular combination of these four match signals, generates one of the three independent trigger signals, TRIGGER 1652, TRIGGER 2654 and TRIGGER 3656. Each of these trigger signals are connected to its corresponding circular buffer, which is one of circular buffer 1662, circular buffer 2664 or circular buffer 3666.

Detailed Description Text (10):
These circular buffers each are connected to a processor bus and continually store valid data from a bus until a trigger signal is detected. Each circular buffer responds to its trigger signal input to stop the storage of data from its particular processor bus. Referring again to FIG. 6, circular buffer 1662 stores data from processor bus A 602 until detecting TRIGGER 1652, circular buffer 2664

stores data from processor bus E 610 until detecting TRIGGER 2654, and circular buffer 3666 stores data from processor bus F 612 until detecting TRIGGER 3656. In this example, data is not stored from processor buses B 604, C 606 and D 608.

Detailed Description Text (11):
After detecting a trigger signal, trace data obtained from a processor bus is retained in a circular buffer until it is uploaded to an external device or until the buffer is reset. Continuing to refer to FIG. 6, bus data is read from circular buffer 1662 via the TRACE OUT 1672 output, bus data is read from circular buffer 2664 via the TRACE OUT 2674 output, and bus data is read from circular buffer 3666 via the TRACE OUT 3676 output.

Detailed Description Text (12):
The bus monitor also provides inputs for trigger conditions, which include bus match and event match conditions, to be downloaded to the bus monitor from an external device. Still referring to FIG. 6, an input downloads data to each of the bus match and event match circuits. In this example, the bus match circuits are chained together with serial data paths BUS MATCH DATA 1-4682-688. Externally originating data specifying a bus match condition is serially shifted onto the TDI 680 line, into and through the Bus Match 1 circuit 622, and onto the BUS MATCH DATA 1682 line. This data continues to shift from the BUS MATCH DATA 1682 line, into and through the Bus Match 2624 circuit, and onto the BUS MATCH DATA 2684 line. As bus match condition data continues to be downloaded to the bus monitor, it shifts from the BUS MATCH DATA 2684 line, into and through the Bus Match 3626 circuit, and onto the BUS MATCH DATA 3686 line. Finally, as bus match conditions continue to be externally downloaded, this data shifts from the BUS MATCH DATA 3686 line and into the Bus Match 4 circuit 628. This downloading process continues until the bus match condition data has been fully shifted into each of the bus match circuits. A BUS MATCH DATA 4688 output data path is optionally provided so that test data can be shifted through the bus match circuits to an external interface so that an external device can verify proper operation of these circuits.

Detailed Description Text (20):
FIG. 8 illustrates a detailed block diagram of a preferred embodiment of an event match circuit. In general, the event match circuit generates a TRIGGER signal 842 on the synchronized occurrence of one or more matching conditions as determined by the bus matching circuits described above. Referring to FIG. 8, the outputs 812 of a don't care register 810 are bit-wise "ORed" 820 with the multiple match signals MATCH1-MATCH4822, which are outputs from the bus match circuits. The outputs 824 of the "OR" 820 are then "ANDed" 830 together. This allows the event match circuit to be configured to ignore the MATCH signals from particular bus match circuits. The output 832 of the "AND" 830 is clocked 712 into a flip-flop 840 to create a single, synchronized TRIGGER signal 842.

Detailed Description Text (22):
One of ordinary skill in the art will recognize that many other embodiments of an event matching circuit having similar functions to the preferred embodiment disclosed above are feasible. Further, embodiments of an event matching circuit having enhanced functions are also feasible. For example, the MATCH signal shown in FIG. 7 could be latched such that it remains asserted until cleared by a reset signal, downloaded instruction or otherwise. In that manner, the TRIGGER signal shown in FIG. 8 could be generated in response to non-simultaneously occurring states occurring on multiple buses.

Detailed Description Text (24):
FIG. 9 illustrates a detailed block diagram of a preferred embodiment of a circular buffer. The circular buffer provides a random access memory, RAM 910 to store bus data. The circular buffer circuitry includes a trigger flip-flop 920 which responds to the occurrence of a TRIGGER signal 842 from a corresponding event match circuit. This flip-flop controls the RAM read/write circuitry. Other circular buffer

circuitry includes an address counter 930 which points to RAM data locations and a shift register 940 which loads bus data read from RAM 910 and outputs that data to an external interface.

Detailed Description Text (25):
The trigger flip-flop 920 controls whether the RAM 910 is writing or reading bus data. Upon a RESET* signal 1374 and until the occurrence of the TRIGGER signal 842, the positive asserted output, Q, 922 and negative asserted output, Q/ 924 of the trigger flip-flop 920 allow writes to RAM by enabling the VALID signal 714 to assert the RAM write enable input 912 and by asserting the enable input 952 of the tri-state buffer 950. The tri-state buffer 950 drives bus data 904 from a DSP bus 902 onto the RAM data lines 914. Upon the occurrence of the TRIGGER signal 842, the trigger flip-flop outputs 922, 924 change states to de-assert the RAM write enable input 912, de-assert the tri-state buffer enable input 952, and assert the RAM read enable input 916, disabling RAM writes and enabling RAM reads. The trigger flip-flop Q output 922 also generates an active STATUS signal 926 which can be read through the external interface as described below. The active STATUS signal 926 allows an external device to determine when a triggering event has occurred in order to initiate an upload of trace data from the circular buffer.

Detailed Description Text (26):
An address counter 930 controls the RAM address lines 932. The counter 930 increments upon the occurrence of a pulse on its clock input 934, generating addresses from the lowest RAM address to the highest RAM address. At the next count after the highest RAM address, the counter overflows to zero, causing the counter to seamlessly wrap back to the lowest RAM address. During data writes from the DSP bus 902 into RAM 910, the source of the count pulse is VALID 714 which is gated to the counter 930 via a multiplexer 960. During data reads from RAM 910, the source of the count pulse is the UPDATEDR-CB signal 1332, which is also gated to the counter 930 via the multiplexer 960. The multiplexer 960 has a select input 962, controlled by the trigger flip-flop Q output 922, which selects the count pulse source as either VALID 714 or UPDATEDR-CB 1332. As stated above, VALID 714 is DSP-derived and indicates when valid data is available on the bus. The UPDATEDR-CB signal 1332 is derived from a signal generated by the external interface, as discussed below. RAM writes are "free-running" such that the circular buffer continuously overwrites itself until the occurrence of a triggering event.

Detailed Description Text (28):
FIG. 10 illustrates how data is stored and retrieved from the circular buffer. The example shown in FIG. 10 depicts a RAM 1000 having 64K (65,536) data cells 1010 with addresses 1020 ranging from 0 to FFFF.sub.16. Before a triggering event, bus data is continuously loaded from the lower to the higher RAM addresses, overwriting previously stored bus data. Assuming a trigger occurs after data was written to RAM address 4FFF.sub.16, then the oldest data 1012 remaining in RAM (i.e., the data written to RAM first compared with all other data remaining in RAM) is at address 5000.sub.16. Data is then read out of RAM beginning with the oldest data 1012 at address 5000.sub.16 and continuing to data 1014 at the highest memory address FFFF.sub.16. At address FFFF.sub.16, the address counter overflows to address 0. Data continues to be read from that data cell 1010 at address 0 through the data cell 1016 at address 4FFF.sub.16, at which point the external interface will have read the entire 64K data cells stored in RAM 1000 and will stop requesting data Thus, a 64K word data trace from a DSP bus will have been captured and uploaded, beginning with the data which occurred on the DSP bus furthest in time from the triggering event and ending with data occurring just prior in time to the triggering event.

Detailed Description Text (32):
The external interface allows trigger conditions to be externally loaded into the bus monitor and provides for the circular buffer contents to be externally read for analysis and display. A preferred embodiment of the external interface is based on

the IEEE Standard Test Access Port and Boundary-Scan Architecture, described in IEEE Std 1149.1-1990. FIG. 11 is a detailed block diagram of the circuitry defined by IEEE Std 1149.1. The test logic shown in FIG. 11 consists of a Test Access Port (TAP) 1110, a TAP controller 1120, an instruction register 1130 and a bank of test data registers 1140.

Detailed Description Text (43):
Referring to FIG. 13, the STATUS[1:3] input 1372 to the instruction register 1130 is from the three circular buffer circuits and comprises one STATUS signal 926 from each trigger flip-flop 920 in a circular buffer circuit, as described above with respect to FIG. 9. The instruction register can capture that status, upon TAP controller assertion of the CAPTURE-IR signal 1122, and that status can be shifted to the external interface output, TDO 1112, to be read by an external device. In this manner, an external device can detect when a trigger condition has occurred, indicating the corresponding circular buffer data is ready to be uploaded. For example, if one bit of the STATUS[1:3] input 1372 indicates that circular buffer 1 has been triggered, the external device then downloads an instruction which specifies circular buffer shift register 11330 to the instruction register 1130. That instruction is decoded 1150, generating a register select input 1368 to the register control 1360 and an output select signal 1369 to the multiplexer 1160 so that CAPTUREDR-CB1 and SHIFTDR-CB1 signals are input to circular buffer shift register 11330 and the TDO-CB1 output 1336 is switched to the multiplexer output 1162 and out to the external device via the second multiplexer 1170, the output buffer 1180 and the TAP output, TDO 1112.

Detailed Description Text (44):
FIG. 14, comprising FIGS. 14A-14M, illustrates the timing associated with initializing bus monitor trigger conditions. Table 1 lists controllers states and associated state codes. As shown in FIG. 14G, an instruction is first downloaded to the instruction register while SHIFTIR is asserted 1410. The downloaded instruction selects a specified test data register to be initialized, that is, the bus match data register or the event match data register. This instruction is loaded into the instruction register on the edge of the UPDATEIR signal 1420, shown in FIG. 14H. Next, as shown in FIG. 14J, trigger conditions are downloaded to the specified test data register while SHIFTDR is asserted 1430. These trigger conditions are latched on the edge of the UPDATEDR signal 1440, shown in FIG. 14K. Two such sequences of loading the instruction register to select a test data register and loading the specified test data register are necessary to load all stages of the bus match data register and event match data register with corresponding mask, bus value, comparator select and don't care data.

Detailed Description Text (46):
The preferred embodiment of the external interface has been disclosed as a serial interface based upon IEEE Std 1149.1. One of ordinary skill in the art, however, will appreciate that many other embodiments of the external interface are feasible. For example, a serial interface which does not necessarily comply with IEEE Std 1149.1 could be implemented to download trigger conditions from an external device and upload bus trace data to an external device. Also, various parallel interface embodiments, although requiring more external pin-outs, could be used to transfer trigger conditions and data to and from the bus monitor of the current invention. For example, the mask, bus value, comparator select, don't care and circular buffer registers could all be implemented as parallel load, parallel output devices interconnected by a common, externally accessible bus. Appropriate control signals could then be used to transfer trigger data into and trace data out of these registers via the common bus.

CLAIMS:

1. A system for monitoring the internal operation of a processor, said processor comprising a plurality of external contacts and one or more internal buses, said

internal buses not accessible from said contacts, said system comprising: an interface connected to at least one of said plurality of external contacts and providing a trigger condition input and a bus trace output; a bus watching circuit having a monitor input connected to at least one of said buses, said bus watching circuit configured to generate a trigger output when a trigger condition derived from said trigger condition input compares to a trigger event occurring on said monitor input, said bus watching circuit further comprising a plurality of logic elements; a circular buffer having a bus data input connected to at least one of said buses, said circular buffer configured to store data from said bus data input in response to said trigger output and to read data to said bus trace output; and a display device configured to read and display data stored in said circular buffer.

3. The system of claim 1, wherein: said bus watching circuit generates said trigger output when a predetermined state occurs on a plurality of processor buses.

4. The system of claim 1, wherein said trigger output is generated when an address detected on said monitor input falls within a predetermined range of addresses specified by said trigger condition input.

5. The system of claim 1, wherein said trigger output is generated when a first pattern of data is detected on said monitor input, said first pattern matching a second pattern specified within said trigger condition input.

7. A bus monitor co-located with a processor module, said module having a plurality of external contacts, said processor having a plurality of buses not all of which are accessible from said external contacts, said monitor comprising: an interface means for providing a trigger condition input and a bus trace output; a bus watching means for monitoring input connected to at least one of a plurality of buses, said bus watching means configured to generate a trigger output only when a trigger condition derived from said trigger condition input compares to a trigger event occurring on a monitor input; and a circular buffer having a means for providing a bus input connected to at least one of said buses, said circular buffer configured to continually store data from said bus data input when said trigger output is present, and to read data to said bus trace output.

8. A bus monitor co-located with a processor on a chip, circuit module or circuit board, said chip, module or board having a plurality of external contacts, said processor having a plurality of buses not all of which are accessible from said contacts, said monitor comprising: an interface connected to at least one of said plurality of external contacts and providing a trigger condition input and a bus trace output; a bus watching circuit having a monitor input connected to at least one of said buses, said bus watching circuit comprising a plurality of logic elements and configured to generate a trigger output when a trigger condition derived from said trigger condition input compares to a trigger event occurring on said monitor input; and a circular buffer which continuously writes data until the occurrence of said trigger output, said circular buffer having a bus data input connected to at least one of said buses and having the ability to be read from and written to via the same port, said circular buffer further being configured to store data from said bus data input in response to said trigger output and to read data to said bus trace output.

9. A bus monitor co-located with a processor on an integrated circuit, said integrated circuit having a plurality of external contacts, said processor having a plurality of buses not all of which are accessible from said contacts, said monitor comprising: an interface connected to at least one of said plurality of external contacts and providing a trigger condition input and a bus trace output; a bus watching circuit having a monitor input connected to at least one of said buses, said bus watching circuit configured to generate a trigger output when a trigger condition derived from said trigger condition input compares to a trigger event occurring on said monitor input, said trigger output no longer being generated when

said trigger condition is no longer satisfied; and a memory having a bus data input connected to at least one of said buses, said memory having the ability to be read from and written to via the same port, and being configured to store data continually from said bus data input in response to said trigger output and to read data to said bus trace output.

10. The monitor of claim 9, wherein: said bus watching circuit generates said trigger output when a predetermined state occurs on a plurality of processor buses.

11. The monitor of claim 9, wherein said trigger output is generated when an address detected on said monitor input falls within a predetermined range of addresses specified by said trigger condition input.

12. The monitor of claim 11, wherein said trigger output is generated when a first pattern of data is detected on said monitor input, said first pattern matching a second pattern specified within said trigger condition input.

13. A system for monitoring the internal operation of a data processing device, said processing device comprising a plurality of external contacts and one or more internal bus means, said internal bus means not accessible from said contacts, said system comprising: interface means connected to at least one of said plurality of external contacts for providing a trigger condition input and a bus trace output; bus watching means having a monitor input connected to at least one of said buses, said bus watching means generating a trigger output when a trigger condition derived from said trigger condition input compares to a trigger event occurring on said monitor input, said bus watching means further comprising a plurality of logic elements; a buffer means having a bus data input connected to at least one of said buses, said buffer means storing data from said bus data input in a predetermined sequential order in response to said trigger output and to read data to said bus trace output; means for reading data stored in said buffer means; and means for displaying said data stored in said buffer means to a user.

Hit List

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Search Results - Record(s) 1 through 10 of 32 returned.

☐ 1. Document ID: US 6026503 A

L2: Entry 1 of 32 File: USPT Feb 15, 2000

US-PAT-NO: 6026503
DOCUMENT-IDENTIFIER: US 6026503 A

TITLE: Device and method for debugging systems controlled by microprocessors

DATE-ISSUED: February 15, 2000

INVENTOR-INFORMATION:

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Treves; Ron	Rechovot			IL
Veisman; Matias	Rechovot			IL
Wohlfarth; Michael	Maale Adumim			IL

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NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
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APPL-NO: 08/ 909817 [PALM]
DATE FILED: August 12, 1997

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US-CL-CURRENT: 714/45; 714/47

FIELD-OF-SEARCH: 395/183.14, 395/184.01, 395/55.1, 395/575, 395/183.04, 395/183.21, 714/25, 714/28, 714/34, 714/38, 714/45, 714/47

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

h e b b cg b e e ch

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5357628	October 1994	Yuen	714/34
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FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
455 946 A2	February 1991	EP	

ART-UNIT: 277

PRIMARY-EXAMINER: Palys; Joseph E.

ASSISTANT-EXAMINER: Nguyen; Nguyen Xuan

ATTY-AGENT-FIRM: Friedman; Mark M.

ABSTRACT:

A device and method for interactively debugging a system controlled by a microprocessor. The device continuously monitors the signals passed along the system bus, watching for signals that match interactively defined break conditions and trace conditions. When a breakpoint condition is satisfied, the device causes the system's microprocessor to execute debug code, which either may mediate interactive control of the system by the user or may initiate the execution of a software patch. When a trace condition is satisfied, the device initiates tracing of bus activity. The device is controlled by the user using conventional interactive interface means such as a video terminal or a personal computer.

23 Claims, 3 Drawing figures

☐ 2. Document ID: US 5999163 A

L2: Entry 2 of 32 File: USPT Dec 7, 1999

US-PAT-NO: 5999163
DOCUMENT-IDENTIFIER: US 5999163 A

TITLE: Digital oscilloscope with high live time recording of signal anomalies and method

DATE-ISSUED: December 7, 1999

INVENTOR-INFORMATION:

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NAME	CITY	STATE	ZIP CODE	COUNTRY
Ivers; Kevin T.	Woodland	WA		
Etheridge; Eric P.	Beaverton	OR		
Siegel; Roy I.	Portland	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Tektronix, Inc.	Wilsonville	OR			02

APPL-NO: 08/ 742544 [PALM]
DATE FILED: November 1, 1996

INT-CL: [06] G09 G 5/36

US-CL-ISSUED: 345/134; 324/121R
US-CL-CURRENT: 345/208; 324/121R

FIELD-OF-SEARCH: 364/487, 324/121R, 345/134, 345/133, 345/135

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4743844	May 1988	Odenheimer et al.	324/121R
4829293	May 1989	Schalter	340/722
5028914	July 1991	Povenmire	340/720
5123034	June 1992	Grujon	377/19
5247287	September 1993	Jonker et al.	345/134
5250935	October 1993	Jonker et al.	345/134
5530454	June 1996	Etheridge et al.	345/134

ART-UNIT: 278

PRIMARY-EXAMINER: Luu; Matthew

ASSISTANT-EXAMINER: Frenel; Vanel

ATTY-AGENT-FIRM: Langlotz; Bennet K. Griffith; Boulden G. Lenihan; Thomas F.

ABSTRACT:

A method of analyzing and displaying waveforms by acquiring an electrical signal, converting it into a stream of digital data points, and sequentially storing each data point to a memory device. Then, analyzing each of the data points to detect whether the data point is an anomalous data point outside of a preselected range. Until an anomalous data point is detected, the steps of acquiring, converting, storing, and analyzing data are repeated. Shortly after the anomalous data point is detected, storage of the data points to the memory device is stopped, so that the anomalous data point and adjacent data points are preserved in memory. Then, the anomalous data point is displayed, preferably along with the immediately preceding and succeeding data points.

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20 Claims, 3 Drawing figures

☐ 3. Document ID: US 5960457 A

L2: Entry 3 of 32 File: USPT Sep 28, 1999

US-PAT-NO: 5960457
DOCUMENT-IDENTIFIER: US 5960457 A

TITLE: Cache coherency test system and methodology for testing cache operation in the presence of an external snoop

DATE-ISSUED: September 28, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Skrovan; Joseph	Buda	TX		
Presley; Royce K.	Kyle	TX		
Carter; Hamilton B.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 08/ 846651 [PALM]
DATE FILED: May 1, 1997

INT-CL: [06] G06 F 12/00

US-CL-ISSUED: 711/146; 711/141, 714/32, 714/33
US-CL-CURRENT: 711/146; 711/141, 714/32, 714/33

FIELD-OF-SEARCH: 711/146, 711/142, 711/143, 711/141, 711/144, 711/145, 395/183.18, 395/425, 395/550, 395/182.03, 395/575, 395/183.05, 364/580, 714/33, 714/42, 714/32, 714/37, 714/708

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5155824	October 1992	Edenfield et al.	
5195089	March 1993	Sindhu et al.	
5197144	March 1993	Edenfield et al.	
5226144	July 1993	Moriwaki et al.	
5317720	May 1994	Stamm et al.	
5325504	June 1994	Tipley et al.	
5341487	August 1994	Derwin et al.	395/425

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5353423	October 1994	Hamid et al.	
5355467	October 1994	MacWilliams et al.	
5355471	October 1994	Weight	395/575
5359723	October 1994	Mathews et al.	
5406504	April 1995	Denisco et al.	364/580
5426765	June 1995	Stevens et al.	
5428761	June 1995	Herlihy et al.	
5740353	April 1998	Kreulen et al.	395/183.18
5748879	May 1998	Kobayashi	395/183.19
5793941	December 1995	Pencis et al.	395/182.03

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 397 995 A2	November 1990	EP	

OTHER PUBLICATIONS

Patent Abstracts of Japan, Publication No. JP5282208, Publication Date Oct. 29, 1993, Application No. JP920081233, Application Date Apr. 3, 1992.
Edenfield, R. et al., "The 68040 On-Chip Memory Subsystem," Institute of Electrical and Electronics Engineers, Feb. 1990, Computer Society International Conference (COMPCON), Spring Meeting, Los Alamitos, No. Conf. 25, pp. 264-269.
Atkins, M., "Performance and the I860 Microprocessor," IEEE Micro, Oct. 1, 1991, vol. 11, No. 5, pp. 24-27, 72-78.
Handy, Jim, "The Cache Memory Book," Academic Press, Inc., San Diego, CA, 1993, pp. 158-190.
European Search Report for EP 95 30 3214.1 dated Aug. 24, 1995.
Hennessy & Patterson, Computer Architecture A Quantitative Approach, 1990 by Morgan Kaufmann Publishers, Inc., pp. 467-474.

ART-UNIT: 271

PRIMARY-EXAMINER: Chan; Eddie P.

ASSISTANT-EXAMINER: McLean; Kimberly Nicole

ATTY-AGENT-FIRM: Conley, Rose & Tayon, PC Kivlin; B. Noel

ABSTRACT:

A test methodology for a cache memory subsystem includes setting a test unit to initiate a snoop cycle on a local bus upon lapse of a predetermined delay. The predetermined delay is initially set to a very short delay or a zero delay. The snoop cycle to be executed may take the form of an inquire cycle to a predetermined memory address. The test unit is further set or programmed to begin monitoring the local bus for certain activity including activity which is indicative of whether the snoop cycle occurred. After programming the test unit, the processor core executes a memory operation associated with the address of the snoop cycle. This memory operation causes a cache line transition. At some point, either before, during or after effectuation of the memory operation, the snoop cycle is executed by the test unit in accordance with the predetermined delay. Upon completing the memory operation, a status register is read from the test unit to determine whether the snoop cycle has yet occurred. If the snoop cycle occurred prior to completing

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the memory operation, the predetermined delay is increased and the test is repeated for the increased delay. Prior to repeating the test, the cache line's coherency with external memory is checked for conformance with the cache protocol. Additionally, the test unit may further be programmed to detect an occurrence of certain external local bus signals generated by the cache memory subsystem, such as a signal indicating a hit to a cache line occurred, and a signal indicating that a hit to a modified line in the cache occurred. The test is repeated until it is determined that the snoop cycle has not occurred upon completion of the line fill instruction.

12 Claims, 5 Drawing figures

☐ 4. Document ID: US 5908392 A

L2: Entry 4 of 32 File: USPT Jun 1, 1999

US-PAT-NO: 5908392
DOCUMENT-IDENTIFIER: US 5908392 A

TITLE: System and method for recording and storing medical data in response to a programmable trigger

DATE-ISSUED: June 1, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wilson; Raymond J.	Parker	CO		
Sloman; Laurence S.	West Hollywood	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Pacesetter, Inc.	Sylmar	CA			02

APPL-NO: 08/ 596895 [PALM]
DATE FILED: March 13, 1996

INT-CL: [06] A61 B 5/0452

US-CL-ISSUED: 600/509; 600/523
US-CL-CURRENT: 600/509; 600/523

FIELD-OF-SEARCH: 600/509, 600/513, 600/515, 600/518, 600/516, 600/517, 600/519, 600/521, 600/522, 600/523, 607/2, 607/4, 607/5, 607/6, 607/9, 607/14, 607/17-26, 607/30, 607/62, 607/32

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL

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4250888	February 1981	Grosskopf	600/515
4295474	October 1981	Fischell	600/509
4966157	October 1990	Suzuki	600/509
5205283	April 1993	Olson	600/518
5513645	May 1996	Jacobson et al.	600/518

ART-UNIT: 377

PRIMARY-EXAMINER: Kamm; William E.

ASSISTANT-EXAMINER: Schaetzle; Kennedy J.

ABSTRACT:

The system of the present invention records and stores, in long-term memory and in form of data snapshots, medical data acquired prior to and subsequent to an occurrence of cardiac episodes and implantable device functions defined as important by the medical practitioner. The system provides the medical practitioner with the ability to specify trigger criteria representative of important cardiac episodes and implantable device functions. The system of the present invention allows the medical practitioner to control the amount of medical data stored in the data snapshots. The system allows the medical practitioner to specify a mode of storing data snapshots when the maximum storage capacity of long-term memory has been reached. In a first mode, the system stores data snapshots in a circular buffer manner, overwriting the older data snapshots. In a second mode, the system stops storing new data snapshots after the maximum storage capacity of long-term memory has been reached.

42 Claims, 11 Drawing figures

☐ 5. Document ID: US 5812830 A

L2: Entry 5 of 32 File: USPT Sep 22, 1998

US-PAT-NO: 5812830
DOCUMENT-IDENTIFIER: US 5812830 A

TITLE: Debug system with raw mode trigger capability

DATE-ISSUED: September 22, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Naaseh-Shahry; Hosein	Windsor	CO		
Tobin; Paul G.	Fort Collins	CO		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA			02

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APPL-NO: 08/ 749863 [PALM]
DATE FILED: November 14, 1996

INT-CL: [06] G06 F 11/00

US-CL-ISSUED: 395/551; 395/557, 395/183.01
US-CL-CURRENT: 713/400; 713/502, 714/25

FIELD-OF-SEARCH: 395/551, 395/557, 395/559, 395/183.01, 395/183.08, 395/183.09, 395/183.13, 395/184.01, 371/22.1, 371/22.6

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4678345	July 1987	Agoston	368/119
4713813	December 1987	Sugimori et al.	371/22.1
4910417	March 1990	El Gamal et al.	307/465
5317711	May 1994	Bourekas et al.	395/425
5375228	December 1994	Leary et al.	395/183.09
5418452	May 1995	Pyle	395/158.1
5473754	December 1995	Folwell et al.	395/183.21
5488688	January 1996	Gonzales et al.	395/183.1

OTHER PUBLICATIONS

U.S. application No. 08/711,491 of Gregory L. Ranson, et al. filed Sep. 10, 1996 for: On-Chip Debug Support and Performance Monitoring in a Microprocessor.

ART-UNIT: 277

PRIMARY-EXAMINER: Heckler; Thomas M.

ABSTRACT:

Disclosed herein is sophisticated but low-cost debug hardware which may be used to identify the root cause of a functional or electrical problem in a microprocessor chip. The debug system comprises a raw mode trigger capability which allows microprocessor events to be generated either synchronously or asynchronously to a clock which steps an instruction pipeline. The debug system comprises one or more trigger means, one or more event generation means, and programmable means for alternately placing the one or more trigger means in synchronous or asynchronous mode. Each of the trigger means is implemented internally to a microprocessor so as to sample microprocessor signals and generate a number of triggers as programmed values of the microprocessor signals are detected. Each of the event generation means is also implemented internally to a microprocessor, and may be used to generate one or more microprocessor events in response to programmed combinations of the number of triggers generated by said trigger means. If desired, generation of a microprocessor event may be delayed until either 1) a programmed trigger combination has occurred a set number of times, or 2) a programmable countdown timer has expired.

20 Claims, 15 Drawing figures

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 6. Document ID: US 5729678 A

L2: Entry 6 of 32 File: USPT Mar 17, 1998

US-PAT-NO: 5729678
DOCUMENT-IDENTIFIER: US 5729678 A

TITLE: Bus monitor system

DATE-ISSUED: March 17, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hunt; Jeffrey Glenn	Glendale	AZ		
Perry; Thomas Jay	Phoenix	AZ		
Gilbert; Michael	Glendale	AZ		
Brown; Randall Lew	Phoenix	AZ		
Southway, Jr.; James B.	Glendale	AZ		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
AG Communication Systems Corporation	Phoenix	AZ			02

APPL-NO: 08/ 611984 [PALM]
DATE FILED: March 4, 1996

INT-CL: [06] G06 F 11/00

US-CL-ISSUED: 395/183.19
US-CL-CURRENT: 714/43

FIELD-OF-SEARCH: 395/183.01, 395/183.16, 395/183.19, 395/473, 395/835, 395/306, 364/264

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4453211	June 1984	Askinazi et al.	
5426741	June 1995	Butts, Jr. et al.	
5471462	November 1995	Amador	370/17

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL

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57-037382	March 1982	JP
1-184992	July 1989	JP
3-014964	January 1991	JP

ART-UNIT: 243

PRIMARY-EXAMINER: DeCady; Albert

ATTY-AGENT-FIRM: Zwick; David J. Hendricks; Gregory G.

ABSTRACT:

A bus monitor system comprises eight identical programmable monitor circuits that are each connected to a monitored bus and to a local 16-bit event bus. There are three interfaces to the event bus within each monitor circuit. One interface asserts a predetermined bit pattern on the event bus when match conditions occur between bit patterns on the monitored bus and predetermined bit patterns stored in monitor circuit registers. A second interface asserts a signal on an external pin when bit patterns on the event bus match a predetermined bit pattern stored in a monitor circuit register. A third interface asserts a predetermined bit pattern on the event bus when an external device has asserted a signal on an external pin. Each monitor circuit is capable of reading and asserting any of the bits of the event bus. The event bus is used to enable or disable monitor circuit interfaces. If any asserted bit on the event bus matches a corresponding bit of one of the predetermined bit patterns stored in the interface enable and disable registers, that interface will be enabled or disabled, respectively. The event bus gives the monitor system the ability to simultaneously monitor for multiple bit patterns on the monitored bus, and to monitor for a sequence of bit patterns by having one monitor circuit trigger another.

7 Claims, 19 Drawing figures

☐ 7. Document ID: US 5671172 A

L2: Entry 7 of 32 File: USPT Sep 23, 1997

US-PAT-NO: 5671172
DOCUMENT-IDENTIFIER: US 5671172 A

TITLE: Method of pedestal and common-mode noise correction for switched-capacitor analog memories

DATE-ISSUED: September 23, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Britton; Charles L.	Alcoa	TN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE

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Lockheed Martin Energy Systems, Inc. Oak Ridge TN 02

APPL-NO: 08/ 738626 [PALM]
DATE FILED: October 29, 1996

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATIONS This application is a divisional application of U.S. patent application Ser. No. 08/316,193 filed on Sep. 30, 1994, now U.S. Pat. No. 5,590,104.

INT-CL: [06] G11 C 27/00

US-CL-ISSUED: 365/45; 365/149, 365/206, 365/210
US-CL-CURRENT: 365/45; 365/149, 365/206, 365/210

FIELD-OF-SEARCH: 365/45, 365/149, 365/206, 365/207, 365/210

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4445189	April 1984	Hyatt	365/45
5388064	February 1995	Khan	365/45

OTHER PUBLICATIONS

J. T. Walker et al, "Microstore --The Stanford Analog Memory Unit", IEEE Trans. Nucl. Sci., vol. NS-32, No. 1, pp. 616-621, Feb. 1985.
W. Sippach et al, "Development of the Front End Electronics for the ZEUS High Resolution Calorimeter," IEEE Trans. Nuc. Sci., NS-36, pp. 465-469, Feb. 1989.
B. Wadsworth, "Technology-Independent Design Considerations for Switched-Capacitor Analog Memories," M.I.T., Laboratory of Nuclear Science Electronics Facility Technical Note 89-6, Jun. 1989.
A. Konstantinidis and B. Wadsworth, "Design Considerations for Switched-Capacitor Analog Memories," 1991 Nuclear Science Symposium and Medical Imaging Con. Record, pp. 606-610, Nov. 2-9, 1991.

ART-UNIT: 251

PRIMARY-EXAMINER: Nelms; David C.

ASSISTANT-EXAMINER: Hoang; Huan

ATTY-AGENT-FIRM: Spicer; James M.

ABSTRACT:

A method and apparatus for correcting common-mode noise and pedestal noise in a multichannel array of switched-capacitor analog memories wherein each analog memory is connected to an associated analog-to-digital converter. The apparatus comprises a single differential element in two different embodiments. In a first embodiment, the differential element is a reference analog memory connected to a buffer. In the second embodiment, the differential dement is a reference analog memory connected to a reference analog-to-digital connected to an array of digital summing circuits.

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3 Claims, 4 Drawing figures

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWIC | Draw De

☐ 8. Document ID: US 5640542 A

L2: Entry 8 of 32 File: USPT Jun 17, 1997

US-PAT-NO: 5640542
DOCUMENT-IDENTIFIER: US 5640542 A
**** See image for Certificate of Correction ****

TITLE: On-chip in-circuit-emulator memory mapping and breakpoint register modules

DATE-ISSUED: June 17, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Whitsel; Ronald J.	Beaverton	OR		
Hobbs; William A.	Beaverton	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 583310 [PALM]
DATE FILED: January 5, 1996

PARENT-CASE:
This is a continuation of application Ser. No. 08/145,757, filed Oct. 29, 1993, now abandoned.

INT-CL: [06] G06 F 9/445

US-CL-ISSUED: 395/500; 395/183.04, 395/183.1
US-CL-CURRENT: 703/28; 714/28, 714/34

FIELD-OF-SEARCH: 395/500, 395/183.04, 395/800, 395/375, 395/183.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4674089	June 1987	Poret et al.	371/25
4740895	April 1988	Sargent et al.	395/183.01
4796258	January 1989	Boyce et al.	395/183.05
4901259	February 1990	Watkins	364/578
4939637	July 1990	Pawloski	395/500
4964074	October 1990	Suzuki et al.	395/500

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5047926	September 1991	Kuo et al.	364/267.91
5056013	October 1991	Yamamoto	364/247.6
5123107	June 1992	Mensch, Jr.	395/800
5132971	July 1992	Oguma et al.	371/16.2
5226047	July 1993	Catlin	371/16.2
5228039	July 1993	Knoke et al.	395/183.04
5280626	January 1994	Kondo et al.	395/500
5313618	May 1994	Pawloski	395/500
5321828	June 1994	Phillips et al.	395/500
5325512	June 1994	Takahashi	395/500
5333307	July 1994	Shirk et al.	395/183.04
5357626	October 1994	Johnson et al.	395/500
5383192	January 1995	Alexander	395/500
5396611	March 1995	Kusuda	395/550
5537536	July 1996	Groves	395/183.04
5539901	July 1996	Ramirez	395/500

OTHER PUBLICATIONS

Designing a VLSI microprocessor for emulation by Rivin, 1990 I.E.E.E publication pp. p5-8.1,p5-8.4.
An In-circuit analyzer for mixed signal digital signal processor by Beline et al, I.E.E.E. publication pp. 1109-1112, (1991).

ART-UNIT: 235

PRIMARY-EXAMINER: Lim; Krisna

ASSISTANT-EXAMINER: Maung; Zarni

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A pair of In-Circuit-Emulator modules are embedded within a microprocessor to implement parts of an In-Circuit-Emulator system. A first In-Circuit-Emulator module, the In-Circuit-Emulator memory mapping module, maps specified physical addresses into a debug memory. The physical addresses mapped into the debug memory are set by programmable registers. The second In-Circuit-Emulator module, the In-Circuit-Emulator breakpoint module, allows the user to set conditions that cause the processor to recognize specific bus events. The In-Circuit-Emulator breakpoint module monitors an internal bus and an internal bus controller. The user can set specific bus event conditions by writing to a set of breakpoint registers in the breakpoint module.

7 Claims, 7 Drawing figures

☐ 9. Document ID: US 5631910 A

L2: Entry 9 of 32 File: USPT May 20, 1997

h e b b cg b e e ch

US-PAT-NO: 5631910
DOCUMENT-IDENTIFIER: US 5631910 A

TITLE: Information processing system provided with self-diagnosing circuit and the self-diagnosing method therefor

DATE-ISSUED: May 20, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nozuyama; Yasuyuki	Tokyo			JP
Kudou; Tsuneaki	Yokohama			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Kabushiki Kaisha Toshiba	Kawasaki			JP	03

APPL-NO: 08/ 243517 [PALM]
DATE FILED: May 16, 1994

PARENT-CASE:
This application is a continuation of application Ser. No. 07/717,349, filed on Jun. 18, 1991, now abandoned.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	2-157493	June 18, 1990
JP	3-136285	June 7, 1991

INT-CL: [06] G06 F 11/00

US-CL-ISSUED: 371/22.1; 395/183.16
US-CL-CURRENT: 714/724; 714/40

FIELD-OF-SEARCH: 371/21.6, 371/22.1, 365/184.01, 365/183.11

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4785416	November 1988	Stringer	371/27
5018145	May 1991	Kikuchi et al.	371/27
5127010	June 1992	Satoh	371/27

OTHER PUBLICATIONS

Digital Logic and Computer Design by M. Morris Mano .COPYRGT.1979 by Prentice-Hall Inc., pp. 510, 511.

ART-UNIT: 243

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PRIMARY-EXAMINER: Canney; Vincent P.

ATTY-AGENT-FIRM: Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

ABSTRACT:

An information processing system composed of a plurality of circuit blocks operative in an normal operation mode and in a self-diagnosis mode comprises: a clock signal generating circuit for generating a basic clock signal in the normal operation mode, and a first clock signal with a period. N times (N=2, 3, . . .) as long as that of the basic clock signal and a second clock signal out of phase from the first clock signal by a delay less than one cycle of the first clock signal in the self-diagnosis mode; a memory for storing microinstructions for self-diagnosis operative in synchronism with the basic clock signal in the normal operation mode, and in synchronism with the first clock signal in the self-diagnosis mode; a decoder for inputting and decoding the mlcroinstructions for self-diagnosis stored in the memory; a test data generating circuit for generating test data in accordance with the decoded results obtained by the decoder in synchronism with the first clock signal at the self-diagnosis mode; first type circuit blocks operative in synchronism with the basic clock in the normal operation mode, for storing test data generated by said test data generating means In synchronism with the second clock and outputting test data therein In synchronism with the first clock In the self-diagnosis mode; second type circuit blocks for outputting output data corresponding to the test data provided in synchronism with the basic clock signal in the normal operation mode, and in synchronism with the first clock in the self-diagnosis mode; and a signature compressing circuit for inputting the test resultant data outputted from the circuit blocks to diagnose the operation of the circuit blocks, in synchronism with the second clock signal in the self-diagnosis mode.

12 Claims, 19 Drawing figures

☐ 10. Document ID: US 5623673 A

L2: Entry 10 of 32 File: USPT Apr 22, 1997

US-PAT-NO: 5623673
DOCUMENT-IDENTIFIER: US 5623673 A

TITLE: System management mode and in-circuit emulation memory mapping and locking method

DATE-ISSUED: April 22, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gephardt; Douglas D.	Austin	TX		
MacDonald; James R.	Buda	TX		
Andrade; Victor F.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE

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Advanced Micro Devices, Inc. Sunnyvale CA 02

APPL-NO: 08/ 279474 [PALM]
DATE FILED: July 25, 1994

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/733; 395/726, 395/739, 395/740, 395/742
US-CL-CURRENT: 710/260; 710/200, 710/266, 710/267, 710/269

FIELD-OF-SEARCH: 395/725, 395/726, 395/733, 395/739, 395/740, 395/742

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5175853	December 1992	Kardach et al.	
5339437	August 1994	Yuen	395/700
5363500	November 1994	Takeda	395/425
5392420	February 1995	Balmer et al.	395/500
5437039	July 1995	Yuen	395/725

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0575171	December 1993	EP	
9117505	November 1991	WO	

ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Travis; John

ATTY-AGENT-FIRM: Kivlin; B. Noel Conley, Rose & Tayon, P.C.

ABSTRACT:

A computer system is provided that includes an interrupt driven system management mode during which system management code is accessed. In one embodiment, a lock-out register is provided to prevent accesses to the system management code while the computer system is operating in its normal mode. In one embodiment, an interrupt control unit is coupled to the ICE interrupt line of the microprocessor core, and controls a memory control unit in accordance with assertions of an external "debug" interrupt signal and an external SMM (system management mode) interrupt signal. If the debug interrupt signal is asserted while the microprocessor core is operating in its normal mode, the interrupt control unit responsively asserts the ICE interrupt signal to the microprocessor core, thereby, causing the microprocessor core to execute ICE code. If, however, the SMM interrupt signal is asserted while the microprocessor core is operating in its normal mode, the interrupt control unit

responsively asserts an ICE interrupt signal which causes the microprocessor core to commence executing the SMM code. Both the SMM code and ICE code may be mapped within a region of system memory which is common to the mapping of a video controller.

11 Claims, 4 Drawing figures

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Terms	Documents
(5142673| 5210862| 5313618| 5325368| 5329471| 5355369| 5371551| 5375228| 5463760| 5488688| 5513338| 5530804| 5535412| 5539901| 5544311| 5546566| 5560036| 5561761| 5566303| 5590354| 5610826| 5621651| 5623673| 5631910| 5640542| 5671172| 5729678| 5812830| 5908392| 5960457| 5999163| 6026503)![pn]	32

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Search Results - Record(s) 11 through 20 of 32 returned.

☐ 11. Document ID: US 5621651 A

L2: Entry 11 of 32 File: USPT Apr 15, 1997

US-PAT-NO: 5621651
DOCUMENT-IDENTIFIER: US 5621651 A

TITLE: Emulation devices, systems and methods with distributed control of test interfaces in clock domains

DATE-ISSUED: April 15, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugar Land	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 08/ 643703 [PALM]
DATE FILED: May 6, 1996

PARENT-CASE:
This application is a Continuation, of application Ser. No. 08/209,127, filed Mar 9, 1994, now abandoned.

INT-CL: [06] G06 F 17/00, G06 F 11/00

US-CL-ISSUED: 364/489; 364/488
US-CL-CURRENT: 703/23; 703/13

FIELD-OF-SEARCH: 364/488, 364/489, 364/490, 364/491, 371/22.3, 371/22.5, 371/27, 395/500

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4633417	December 1986	Wilburn et al.	364/578
4901259	February 1990	Watkins	364/578

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5126966	June 1992	Hafeman et al.	364/578
5307285	April 1994	Storandt et al.	364/489
5329471	July 1994	Swoboda et al.	364/578
5331571	July 1994	Aronoff et al.	364/490
5388060	February 1995	Adams, Jr. et al.	364/578
5461573	October 1995	Chakradhar et al.	364/489
5479355	December 1995	Hyduke	364/488

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0411904A2	February 1991	EP	

ART-UNIT: 234

PRIMARY-EXAMINER: Trans; Vincent N.

ATTY-AGENT-FIRM: Stahl; Scott B. Heiting; Leo N. Donaldson; Richard L.

ABSTRACT:

An emulation device (11) distributes common control information (8801) to each of a plurality of clock domains (1213, 1215, 1217) into which the emulation device is partitioned, and also provides the clock domains with individualized clock control (8905, 8907, 8913).

12 Claims, 94 Drawing figures

☐ 12. Document ID: US 5610826 A

L2: Entry 12 of 32 File: USPT Mar 11, 1997

US-PAT-NO: 5610826
DOCUMENT-IDENTIFIER: US 5610826 A

TITLE: Analog signal monitor circuit and method

DATE-ISSUED: March 11, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Whetsel; Lee D.	Plano	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

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APPL-NO: 08/ 242155 [PALM]
DATE FILED: May 13, 1994

PARENT-CASE:
This application is a Continuation of application Ser. No. 07/693,756 filed Apr. 30, 1991, now abandoned.

INT-CL: [06] G01 R 31/3163

US-CL-ISSUED: 364/487
US-CL-CURRENT: 702/117

FIELD-OF-SEARCH: 371/22.3, 371/22.4, 371/22.5, 371/25.1, 324/73.1, 324/113, 364/487

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4340857	July 1982	Fasang	371/22.5
4441183	April 1984	Dussault	371/22.4
4524444	June 1985	Efron et al.	324/73.1 X
4634970	January 1987	Payne et al.	324/121R
4903022	February 1990	Hester et al.	341/120 X
4908621	March 1990	Pelonio et al.	341/120
4922492	May 1990	Fasang et al.	371/22.1
4924468	May 1990	Horak et al.	371/221
5081592	January 1992	Jenq	364/487
5185883	February 1993	Ianni et al.	371/21.2 X

OTHER PUBLICATIONS

D. Sheingold, ed., Analog-Digital Conversion Handbook, Prentice-Hall, 1986, pp. 420-427.
Nicholson, B., "Extending Signature Analysis", Electronics Industry, Mar. 1981, pp. 12-16.

ART-UNIT: 236

PRIMARY-EXAMINER: Baker; Stephen M.

ATTY-AGENT-FIRM: Barndt; B. Peter Telecky, Jr.; Frederick J. Donaldson; Richard L.

ABSTRACT:

An analog signal monitoring (ASM) circuit (40, 42) non-intrusively monitors an analog circuit (20) within an electronic system. The ASM circuit (40,42) comprises input circuitry (80) that receives a plurality of analog signal inputs while the analog circuit (20) operates in a functional mode. Translation circuitry (142) associates with the input circuitry (80) for converting the analog signal inputs into digital signal representations of the analog signal inputs. Output circuitry (58) associates with the translation circuitry to output the digital representations. Control circuitry (114) controls the translation and output circuitry while the analog circuit (20) is in a functional mode. The ASM circuit

(40, 42) also include an event qualification circuit (68) that includes input circuitry (236) to receive the digital signal representations, compare circuitry (104) to compare the received digital representations to an expected value and output a matched signal when a compared condition is identified.

23 Claims, 11 Drawing figures

☐ 13. Document ID: US 5590354 A

L2: Entry 13 of 32 File: USPT Dec 31, 1996

US-PAT-NO: 5590354
DOCUMENT-IDENTIFIER: US 5590354 A
**** See image for Certificate of Correction ****

TITLE: Microcontroller provided with hardware for supporting debugging as based on boundary scan standard-type extensions

DATE-ISSUED: December 31, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Klapproth; Peter	Eindhoven			NL
Zandveld; Frederik	Eindhoven			NL
Bakker; Jacobus M.	Eindhoven			NL
Van Loo; Gerardus C.	Eindhoven			NL

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
U.S. Philips Corporation	New York	NY			02

APPL-NO: 08/ 281964 [PALM]
DATE FILED: July 28, 1994

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
EP	93202228	July 28, 1993

INT-CL: [06] G06 F 11/00

US-CL-ISSUED: 395/800; 395/183.06, 371/22.3, 364/232.8, 364/267.91, 364/DIG.1
US-CL-CURRENT: 714/30; 714/727

FIELD-OF-SEARCH: 395/800, 395/500, 395/250, 395/182.08, 395/182.19, 395/183.01, 395/183.04, 395/183.06, 395/183.11, 395/183.13, 371/3, 371/21.3, 371/21.6, 371/22.3, 371/23, 371/29.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4788683	November 1988	Hester et al.	395/183.06
5058114	October 1991	Kuboki et al.	395/183.14
5355369	October 1994	Greenbergerl et al.	371/22.3
5377198	December 1994	Simpson et al.	371/22.3
5381420	January 1995	Henry	371/22.3
5400345	March 1995	Ryan, Jr.	371/22.3
5428623	June 1995	Rahman et al.	371/22.3
5444859	August 1995	Baker et al.	395/182.18
5515382	May 1996	Lassorie	371/22.3

OTHER PUBLICATIONS

"DSD Development Tools Engage Mainstream Designers" K. Marrin, Computer Design, vol. 32, No. 1, Jan. 1993.

ART-UNIT: 232

PRIMARY-EXAMINER: Shah; Alpesh M.

ATTY-AGENT-FIRM: Gathman; Laurie E.

ABSTRACT:

A microprocessor includes a processor element, a memory interface element, an IO interface element, a debug support element and an internal bus interconnecting all above elements. For easy debugging, it also includes attached to the internal bus a registered boundary scan standard (JTAG) interface that accesses one or more scan chains inside the microprocessor, and is arranged for controlling DMA-type exchanges via the internal bus with other elements connected to this bus.

10 Claims, 6 Drawing figures

☐ 14. Document ID: US 5566303 A

L2: Entry 14 of 32 File: USPT Oct 15, 1996

US-PAT-NO: 5566303
DOCUMENT-IDENTIFIER: US 5566303 A

TITLE: Microcomputer with multiple CPU'S on a single chip with provision for testing and emulation of sub CPU's

DATE-ISSUED: October 15, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tashiro; Tetsu	Itami			JP

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Cho; Yoshiki Itami JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 08/ 251556 [PALM]
DATE FILED: May 31, 1994

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	5-128888	May 31, 1993
JP	6-105768	May 19, 1994

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/280; 395/421.03, 395/800, 377/39
US-CL-CURRENT: 710/100; 377/39, 711/213

FIELD-OF-SEARCH: 395/775, 395/280, 395/421.03, 395/800, 377/39

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4296467	October 1981	Nibby, Jr. et al.	364/200
4612631	September 1986	Ochii	365/203
4680701	July 1987	Cochran	364/200
4698750	October 1987	Wilkie et al.	364/200
4796099	January 1989	Comptom	358/342
4799144	January 1989	Parruck et al.	364/200
4977494	December 1990	Gabaldon et al.	364/167.01
5032983	July 1991	Fu et al.	364/200
5121498	June 1992	Gilbert et al.	395/700
5261095	November 1993	Crawford et al.	395/650
5287515	February 1994	Murai	395/700
5367550	November 1994	Ishida	377/39
5410718	April 1995	Masumura et al.	395/800

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
3903835	August 1989	DE	

OTHER PUBLICATIONS

David Jones, "Fehlertoleranz und Zuverlassigkeit in Mikroprozessor-Systemen", Elektronik 24/1990, pp. 54-60.

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ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Travis; John

ATTY-AGENT-FIRM: Lowe, Price, LeBlanc & Becker

ABSTRACT:

A control circuit is provided which enables the main CPU 23 to access a memory space of the sub CPU 1 by means of the test mode control register 4 which can be controlled via the main CPU bus 10. Also a control circuit is provided to branch into a break routine by comparing the value of the program counter 5 of the sub CPU 1 and the value set in the break vector register 7. Further, a control circuit which enables it to reset the sub CPU 1, to branch according to a test vector and to make break branch under the control of the main CPU 23 is provided, thereby making it easy to incorporate the sub CPU 1 on-chip in the conventional single CPU constitution. Thus testing environment and debugging environment for the sub CPU 1 is provided in the microcomputer having a plurality of CPUs on a single chip without connecting the exclusive test terminal of the sub CPU 1 or the sub CPU bus 28 with the outside.

2 Claims, 63 Drawing figures

☐ 15. Document ID: US 5561761 A

L2: Entry 15 of 32 File: USPT Oct 1, 1996

US-PAT-NO: 5561761
DOCUMENT-IDENTIFIER: US 5561761 A

TITLE: Central processing unit data entering and interrogating device and method therefor

DATE-ISSUED: October 1, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hicok; Gary D.	Mesa	AZ		
Lehman; Judson A.	Scottsdale	AZ		
Alexander; Thomas	Hillsboro	OR		
Lim; Yong J.	Seattle	WA		
Evoy; David R.	Tempe	AZ		
Kim; Yongmin	Seattle	WA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
YLSI Technology, Inc.	San Jose	CA			02

APPL-NO: 08/ 522856 [PALM]
DATE FILED: September 1, 1995

PARENT-CASE:
This is a continuation of application Ser. No. 08/040,862 filed on Mar. 31, 1993, now abandoned.

INT-CL: [06] G06 F 11/00

US-CL-ISSUED: 395/183.06; 395/183.16, 395/183.1
US-CL-CURRENT: 714/30; 714/34, 714/40

FIELD-OF-SEARCH: 395/183.06, 395/183.07, 395/183.08, 395/183.1, 395/184.01, 395/183.16

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4899306	February 1990	Greer	371/16.1
4926363	May 1990	Nix	371/20.1
4982402	January 1991	Beaven et al.	371/16.1
5021997	June 1991	Archie et al.	371/16.1
5033047	July 1991	Uehara	371/16.1
5157781	October 1992	Harwood et al.	395/575
5163052	November 1992	Evans et al.	371/16.1
5226149	July 1993	Yoshida et al.	395/575
5228139	July 1993	Miwa et al.	395/575
5274797	December 1993	Barlow et al.	395/575
5276857	January 1994	Hartung et al.	395/575

OTHER PUBLICATIONS

Immaneni et al "Direct Access Test Scheme-Design of Block and Core Cells for Embedded ASICS" 1990 Int. Test Conference IEEE pp. 488-492.
Immaneni et al. "Direct Access Test Scheme-Implementation and Verification in Embedded ASIC Designs" 1990 IEEE ASIC Semirar+Exhibit.

ART-UNIT: 243

PRIMARY-EXAMINER: Beausoliel, Jr.; Robert W.

ASSISTANT-EXAMINER: Palys; Joseph E.

ATTY-AGENT-FIRM: Harry M. Weiss & Associates

ABSTRACT:

A Central Processing Unit (CPU) debugging device and method therefor is disclosed which provides data entering and interrogating devices which will temporarily stop all CPU execution when desired by a user and allow a non-destructive intrusion into the contents of any of the CPU internal registers, state bits, and cache and local

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memories. After the desired CPU contents have been reviewed and subsequently altered or maintained by a user, the CPU execution may be resumed.

16 Claims, 3 Drawing figures

☐ 16. Document ID: US 5560036 A

L2: Entry 16 of 32 File: USPT Sep 24, 1996

US-PAT-NO: 5560036
DOCUMENT-IDENTIFIER: US 5560036 A

TITLE: Data processing having incircuit emulation function

DATE-ISSUED: September 24, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yoshida; Toyohiko	Itami			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 08/ 432316 [PALM]
DATE FILED: May 1, 1995

PARENT-CASE:
This is a continuation of application Ser. No. 08/220,414, filed Mar. 30, 1994, now abandoned, which is a continuation of application Ser. No. 07/624,026, filed Dec. 7, 1990, now abandoned.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	1-326292	December 14, 1989

INT-CL: [06] G06 F 1/00

US-CL-ISSUED: 395/800; 395/375, 395/497.01, 364/231.8, 364/243.2, 364/245.4, 364/260, 364/DIG.1
US-CL-CURRENT: 712/227; 711/170

FIELD-OF-SEARCH: 395/800, 395/425, 395/375, 395/497.01, 364/231.8, 364/243.2, 364/245.4, 364/260, 364/DIG.1

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4674089	June 1987	Poret et al.	371/25
4783731	November 1988	Miyazaki et al.	395/425
4799215	January 1989	Suzuki	370/60
4827402	May 1989	Wada	364/200
4985825	January 1991	Webb, Jr. et al.	395/425
5043870	August 1991	Ditzel et al.	364/200
5056013	October 1991	Yamamoto	395/500
5091853	February 1992	Watanabe et al.	395/375
5136696	August 1992	Beckwith et al.	395/375
5193205	March 1993	Matsuo	395/800
5287483	February 1994	Utsumi	395/425

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
61-241841	October 1986	JP	
63-193230	August 1988	JP	

ART-UNIT: 232

PRIMARY-EXAMINER: Bowler; Alyssa H.

ASSISTANT-EXAMINER: Harrity; John

ATTY-AGENT-FIRM: Towsend and Townsend and Crew LLP

ABSTRACT:

An improved data processor includes a high-speed memory that functions as a data cache during normal operation and as a trace memory to debug software in an in-circuit emulation mode. A register counts the number of storage location and overflows when a predetermined number is exceeded to cause an exception which transfers information off-chip from the trace memory. In one embodiment a starting address is stored and compared to a program counter of an instruction completely executed in the execution unit to begin the tracing.

23 Claims, 35 Drawing figures

☐ 17. Document ID: US 5546566 A

L2: Entry 17 of 32 File: USPT Aug 13, 1996

US-PAT-NO: 5546566
DOCUMENT-IDENTIFIER: US 5546566 A

TITLE: Emulation system for microcomputer

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DATE-ISSUED: August 13, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Katsuta; Hiroshi	Tokyo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
NEC Corporation	Tokyo			JP	03

APPL-NO: 08/ 271506 [PALM]
DATE FILED: July 7, 1994

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	5-191790	July 7, 1993

INT-CL: [06] G06 F 9/455

US-CL-ISSUED: 395/500
US-CL-CURRENT: 703/28

FIELD-OF-SEARCH: 395/500, 395/800, 364/200, 364/488, 364/489, 364/490, 364/491, 364/578, 371/25

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4527234	July 1985	Bellay	364/200
4674089	June 1987	Poret et al.	371/25
5062034	October 1991	Bakker	364/200
5101498	March 1992	Ehlig et al.	395/800
5331571	July 1994	Aronoff et al.	364/490
5339262	August 1994	Rostoker et al.	364/578
5432708	July 1995	Mohsen	364/490

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
2691817A1	December 1993	FR	
2696561A1	April 1994	FR	
358141	March 1991	JP	

OTHER PUBLICATIONS

European Search Report EP 94 11 0607, dated Sep. 28, 1994.
"In Circuit-Emulation in ASIC Architectural Core Designs", by D. Pasternak and T.

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Hike, IEEE, CH1234-5/89/0000, 1989, pp. 6-4.1-6-4.4.
"Computer-Aided Prototyping for ASIC-Based Systems", by S. Walters, IEEE Design and Test of Computers, 0740-7475/91/0006, 1991, pp. 4-10.
"High-Level Synthesis applied to an ASIC Emulation Board", by N. Wehn et al., IEEE, 0-8186-2845-6/92, 1992, pp. 59-64.
"High-Level Synthesis in a Rapid Prototype Environment for Mechatronic System", by N. Wehn et al., IEEE, 0-8186-2780-8/92, 1992, pp. 188-193.
"A Validation Strategy for Embedded Core ASICS", by R. Hasslen and N. Zafar, IEEE, TH303-8/90/0000, 1990, pp. 5-3.1 -5-3.2.
"Logic Cell Emulation for ASIC In-Circuit Emulators", by S. Cravatta, IEEE, TH303-8/90/0000, 1990, pp. 5-2.1-5-2.4.

ART-UNIT: 234

PRIMARY-EXAMINER: Teska; Kevin

ASSISTANT-EXAMINER: Frejd; Russell W.

ATTY-AGENT-FIRM: Whitham, Curtis, Whitham & McGinn

ABSTRACT:

An emulation system for emulating an application specific integrated circuit (ASIC) type microcomputer including a central processing unit, a user specific peripheral function unit and a user specific logic circuit, which are integrated together on a single chip. The emulation system includes a first integrated circuit for emulating the central processing unit, and second and third integrated circuits each of which comprises the ASIC-type microcomputer. Each of the second and third integrated circuits can selectively operate in a first evaluation chip mode in which the central processing unit and the user specific logic circuit are isolated from an internal bus, and in a second evaluation chip mode in which the central processing unit and the user specific peripheral function unit are isolated from the internal bus. The first integrated circuit is connected through an peripheral bus to the internal bus of each of the second and third integrated circuits. The second integrated circuit is put in the first evaluation chip mode for emulating the peripheral function unit, and the third integrated circuit is put in the second evaluation chip mode for emulating the logic circuit.

10 Claims, 4 Drawing figures

☐ 18. Document ID: US 5544311 A

L2: Entry 18 of 32 File: USPT Aug 6, 1996

US-PAT-NO: 5544311
DOCUMENT-IDENTIFIER: US 5544311 A

TITLE: On-chip debug port

DATE-ISSUED: August 6, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY

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Harenberg; Donald D.	Placentia	CA
Watson; George A.	Fullerton	CA
Bindloss; Keith M.	Irvine	CA
Folwell; Dale E.	Placentia	CA

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Rockwell International Corporation	Seal Beach	CA			02

APPL-NO: 08/ 526472 [PALM]
DATE FILED: September 11, 1995

PARENT-CASE:
The following co-pending U.S. patent applications disclose various aspects of an on-chip debug circuit and are hereby included in their entirety by reference: (i) Ser. No. 08/079,580 filed on Jun. 21, 1993, entitled "Debugging Marker System," by Watson, Bindloss, and Folwell, and (ii) Ser. No. 08/155,891, filed Nov. 23, 1993, entitled "Branch Decision Encoding Scheme," by Folwell, Clark, and Harenberg. All cited pending applications are commonly assigned with this application.

INT-CL: [06] G06 F 11/00

US-CL-ISSUED: 395/183.16; 395/183.06
US-CL-CURRENT: 714/40; 714/30

FIELD-OF-SEARCH: 395/183.16, 395/183.06, 395/185.03, 395/185.04, 395/183.13, 395/183.21, 371/22.1, 371/22.5, 371/22.6

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4641308	February 1987	Sacarisen et al.	395/183.06
5053949	October 1991	Allison et al.	364/200
5084814	January 1992	Vaglica et al.	395/325
5088027	February 1992	Tanagawa et al.	395/183.03
5157781	October 1992	Harwood et al.	395/183.06
5253255	October 1993	Carbine	395/183.06
5416919	May 1995	Ogino et al.	395/183.06
5473754	December 1995	Folwell et al.	395/183.21
5479652	December 1995	Dreyer et al.	395/183.06
5491793	February 1996	Somasundaram et al.	395/183.21

ART-UNIT: 243

PRIMARY-EXAMINER: Beausoliel, Jr.; Robert W.

ASSISTANT-EXAMINER: Palys; Joseph E.

ATTY-AGENT-FIRM: Montanye; George A. Arthur; David J.

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ABSTRACT:

A debug port in accordance with the invention provides circuitry for enabling system (hardware and software) development within an inaccessible computer processor. In one embodiment, a debug port is incorporated within the internal logic of a single-chip, reduced instruction set signal processor referred to as the signal processor. A fully implemented debug port is comprised of five interacting functional elements: debug bus unit (DBU), debug command unit (DCU), debug instruction Unit (DIU), debug inject/extract unit (DJU), and a debug flow unit (DFU). The DBU provides circuitry for buffering data received from the signal processor and other functional elements within the debug port as well as accepting data from an external source. The DBU provides for off-chip connections. The DCU provides circuitry for decoding and executing debug commands received by the debug port. The DIU provides circuitry to insert one or more instructions with, or without, data into the instruction stream of the signal processor. The DJU provides circuitry for injecting external sources of information (e.g., an analog input signal, external control signals, or repetitious data signals) into the signal processor under program control. The DFU provides circuitry for monitoring program/task execution.

50 Claims, 6 Drawing figures

☐ 19. Document ID: US 5539901 A

L2: Entry 19 of 32 File: USPT Jul 23, 1996

US-PAT-NO: 5539901
DOCUMENT-IDENTIFIER: US 5539901 A

TITLE: Method and apparatus for system management mode support for in-circuit emulators

DATE-ISSUED: July 23, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ramirez; Jose	Aloha	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 375515 [PALM]
DATE FILED: January 18, 1995

PARENT-CASE:
This is a continuation of application Ser. No. 08/130,115, filed Sep. 30, 1993.

INT-CL: [06] G06 F 11/00

US-CL-ISSUED: 395/500; 364/DIG.1, 364/DIG.2, 364/264, 364/264.3, 364/948.2, 364/948.8

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US-CL-CURRENT: 703/28

FIELD-OF-SEARCH: 364/DIG.1MSFile, 364/DIG.2MSFile, 364/514A, 364/530, 364/800, 364/801, 364/578, 395/500, 395/750

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4631701	December 1986	Kappeler et al.	395/425
4789924	December 1988	Fukuta	371/16.2
4860247	August 1989	Uchida et al.	395/153
4903218	February 1990	Longo et al.	395/157
4937036	June 1990	Beard et al.	345/156
4958303	September 1990	Assarpour et al.	395/163
4989207	January 1991	Polstra	371/16.2
4993027	February 1991	McGraw et al.	371/16.2
5053949	October 1991	Allison et al.	395/375
5056033	October 1991	Hill	364/483
5072412	December 1991	Henderson, Jr. et al.	395/159
5119319	June 1992	Tanenbaum	364/514A
5132971	July 1992	Oguma et al.	371/16.2
5202976	April 1993	Hansen et al.	395/500
5228039	July 1993	Knoke et al.	371/19
5239642	August 1993	Gutierrez et al.	395/425
5313618	May 1994	Pawloski	395/500
5392420	February 1995	Balmer et al.	395/500

ART-UNIT: 235

PRIMARY-EXAMINER: Harrell; Robert B.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

An in-circuit emulation unit with a probe implemented on a microprocessor whilst in emulation upon entering or leaving system management mode. The present invention is used on a microprocessor in a target computer system. The present invention offers the ability to implement a capability where a user could access emulation information while a system is in or out of system management mode. The present invention provides a better way of controlling a target computer system when in system management mode thereby allowing user access to special system management code, processor contents, processor registers and system state variables necessary for debug and design of system management features available on todays laptop and desktop computers.

9 Claims, 5 Drawing figures

☐ 20. Document ID: US 5535412 A

L2: Entry 20 of 32 File: USPT Jul 9, 1996

US-PAT-NO: 5535412
DOCUMENT-IDENTIFIER: US 5535412 A

TITLE: Circular buffer controller

DATE-ISSUED: July 9, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nadehara; Kouhei	Tokyo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
NEC Corporation	Tokyo			JP	03

APPL-NO: 08/ 520182 [PALM]
DATE FILED: August 28, 1995

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	6-201653	August 26, 1994

INT-CL: [06] G06 F 12/02

US-CL-ISSUED: 395/800; 364/238.8, 364/238.6, 364/238.7, 364/DIG.1, 395/437
US-CL-CURRENT: 711/110

FIELD-OF-SEARCH: 395/800, 395/459, 395/437

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4513392	April 1985	Shenk	395/437
5043870	August 1991	Ditzel	395/459
5295250	March 1994	Komoto	395/437
5301336	April 1994	Kodosky	395/800
5388238	February 1995	McHarg	395/437
5463749	October 1995	Wertheizer	395/437

OTHER PUBLICATIONS

J. L. Hennessy and D. A. Patternson, "Computer Architecture: A Quantitative

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Approach," Morgan Kaufmann Publishers, Inc., CA, 1990, pp. 160-167.

ART-UNIT: 232

PRIMARY-EXAMINER: Coleman; Eric

ATTY-AGENT-FIRM: Sughrue, Mion, Zinn, Macpeak & Seas

ABSTRACT:

From a data memory, there is obtained data at an address indicated by the sum of the values respectively of a base register, an index register, and an offset. The data is stored in a data register. A wrap-around process is executed after an arithmetic operation is conducted by an arithmetic unit n times, n being specified by the value loaded in a block-length register. When the value of the index register is equal to or more than that of the element number register, the value of the element number register is subtracted from that of the index register. Since there exists a chance in which arithmetic operation is achieved beyond a circular buffer area allocated in the data memory, a copy of the first portion of the circular buffer is provided after the circular buffer area. Only one wrap-around process is executed each time a plurality of arithmetic operations are conducted, thereby implementing a high-speed circular buffer.

3 Claims, 10 Drawing figures

Terms	Documents
(5142673| 5210862| 5313618| 5325368| 5329471| 5355369| 5371551| 5375228| 5463760| 5488688| 5513338| 5530804| 5535412| 5539901| 5544311| 5546566| 5560036| 5561761| 5566303| 5590354| 5610826| 5621651| 5623673| 5631910| 5640542| 5671172| 5729678| 5812830| 5908392| 5960457| 5999163| 6026503)![pn]	32

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Search Results - Record(s) 21 through 30 of 32 returned.

☐ 21. Document ID: US 5530804 A

L2: Entry 21 of 32 File: USPT Jun 25, 1996

US-PAT-NO: 5530804
DOCUMENT-IDENTIFIER: US 5530804 A

TITLE: Superscalar processor with plural pipelined execution units each unit selectively having both normal and debug modes

DATE-ISSUED: June 25, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Edgington; Gregory C.	Scottsdale	AZ		
Circello; Joseph C.	Phoenix	AZ		
McCarthy; Daniel M.	Phoenix	AZ		
Duerden; Richard	Scottsdale	AZ		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Motorola, Inc.	Schaumburg	IL			02

APPL-NO: 08/ 242767 [PALM]
DATE FILED: May 16, 1994

INT-CL: [06] G06 F 11/26

US-CL-ISSUED: 395/183.06; 395/500, 395/800, 395/550
US-CL-CURRENT: 714/30; 703/28, 712/23, 712/43

FIELD-OF-SEARCH: 395/500, 395/575, 395/700, 395/800, 395/183, 395/.06, 395/550

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4787031	November 1988	Karger et al.	395/800
4924382	May 1990	Shouda	395/700
5193181	March 1993	Barlow et al.	395/181

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5210864	May 1993	Yoshida	395/183.13
5249266	September 1993	Dye et al.	395/162
5313618	May 1994	Pawloski	395/500
5321828	June 1994	Phillips et al.	395/500
5410685	April 1995	Banda et al.	395/183.14

ART-UNIT: 235

PRIMARY-EXAMINER: Kim; Ken S.

ATTY-AGENT-FIRM: Witek; Keith E.

ABSTRACT:

A processor (10) has two modes of operation. One mode of operation is a normal mode of operation wherein the processor (10) accesses user address space or supervisor address space to perform a predetermined function. The other mode of operation is referred to as a debug, test, or emulator mode of operation and is entered via an exception/interrupt. The debug mode is an alternate operational mode of the processor (10) which has a unique debug address space which executes instructions from the normal instruction set of the processor (10). Furthermore, the debug mode of operation does not adversely affect the state of the normal mode of operation while executing debug, test, and emulation commands at normal processor speed. The debug mode is totally non-destructive and non-obtrusive to the "suspended" normal mode of operation. While in debug mode, the existing processor pipelines, bus interface, etc. are utilized.

42 Claims, 12 Drawing figures

☐ 22. Document ID: US 5513338 A

L2: Entry 22 of 32 File: USPT Apr 30, 1996

US-PAT-NO: 5513338
DOCUMENT-IDENTIFIER: US 5513338 A
**** See image for Certificate of Correction ****

TITLE: Apparatus for tracing activity on a bus of an in-circuit emulator

DATE-ISSUED: April 30, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Alexander; James W.	Hillsboro	OR		
Danowski; Terri A.	Aloha	OR		
Peters; Stephen J.	Aloha	OR		
Whitsel; Ronald J.	Beaverton	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE

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Intel Corporation Santa Clara CA 02

APPL-NO: 08/ 030801 [PALM]
DATE FILED: March 12, 1993

INT-CL: [06] G06 F 11/00, G06 F 13/00

US-CL-ISSUED: 395/500; 395/183.19, 395/550
US-CL-CURRENT: 703/28; 713/400, 714/43

FIELD-OF-SEARCH: 395/500, 395/550, 395/183.01, 395/183.09, 395/183.15, 395/183.19, 371/16.2

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4674089	June 1987	Poret et al.	371/16.2
5313618	May 1994	Pawloski	395/500

ART-UNIT: 236

PRIMARY-EXAMINER: Kriess; Kevin A.

ASSISTANT-EXAMINER: Butler; Dennis M.

ATTY-AGENT-FIRM: Lamb; Owen L.

ABSTRACT:

An in-circuit emulator trace bus clocking mechanism. A synchronization clock associated with the trace bus is provided. Arrival of a first event on a microprocessor bus to be traced is signified by a transition of a control line. A start of cycle event is detected. A start of cycle signal is generated with respect to the start of cycle event. A two stage pipeline having stage 1 storage elements and stage 2 storage elements are connected to receive data from the microprocessor bus. The start of cycle signal is used to sample data from the microprocessor bus into the stage 1 storage elements. An end of cycle event is detected. An end of cycle signal is generated with reference to the end of cycle event. The end of cycle signal is used to sample data from the stage 1 storage elements into the stage 2 storage elements. The end of cycle signal is also used to sample data appearing on the microprocessor bus at the end of the cycle into the stage 2 storage elements. The synchronization clock is combined with the end of cycle signal to generate a trace bus valid signal.

24 Claims, 3 Drawing figures

☐ 23. Document ID: US 5488688 A

L2: Entry 23 of 32 File: USPT Jan 30, 1996

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US-PAT-NO: 5488688
DOCUMENT-IDENTIFIER: US 5488688 A

TITLE: Data processor with real-time diagnostic capability

DATE-ISSUED: January 30, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gonzales; David R.	Austin	TX		
Carichner; Gordon A.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Motorola, Inc.	Schaumburg	IL			02

APPL-NO: 08/ 220329 [PALM]
DATE FILED: March 30, 1994

INT-CL: [06] G06 F 11/34

US-CL-ISSUED: 395/183.1
US-CL-CURRENT: 714/34

FIELD-OF-SEARCH: 395/575, 395/325, 395/183.10, 395/183.14, 395/183.15, 395/183.16, 371/16.1, 371/16.2, 371/15.1, 371/19

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4674089	June 1987	Poret et al.	371/25
4813009	March 1989	Tallman	364/900
4881228	November 1989	Shouda	371/19
4924382	May 1990	Shouda	364/200
5047926	September 1991	Kuo et al.	364/200
5053949	October 1991	Allison et al.	364/200
5067073	November 1991	Andrews	395/375
5073968	December 1991	Morrison	395/500
5084814	January 1992	Vaglica et al.	395/325
5257269	October 1993	Hamauchi	371/29.5
5349687	September 1994	Ehlig et al.	395/800
5361348	November 1994	Nakamoto	395/575

OTHER PUBLICATIONS

Sasaki et al.; "16 bit High-Speed DSP .mu.PD77016;" NEC IC Microcomputer Sys., Ltd.; vol. 46, No. 2, pp. 75-78 (1993).
Steven H. Leibson; "In-Circuit emulators for .mu.Cs;" EDN; pp. 64-78 (1989).
Hunter Goatley; "The VMS Watchpoint Utility: Part I;" Perceptics Corp.; pp. 22-25

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(1990).

ART-UNIT: 243

PRIMARY-EXAMINER: Beausoliel, Jr.; Robert W.

ASSISTANT-EXAMINER: Chung; Phung My

ATTY-AGENT-FIRM: Polansky; Paul J.

ABSTRACT:

A data processor (20) includes a diagnostic circuit (23) with a first-in, first-out memory (FIFO) (25) for storing sequential states of an internal bus, such as a program address bus. In one mode, the diagnostic circuit (23) halts a central processing unit (CPU) (21) and the FIFO (25) on the occurrence of an event condition, such as a hardware breakpoint. In a second mode, the diagnostic circuit (23) halts the FIFO (25) but keeps the CPU (21) in normal operation. Thus, the contents of the FIFO (25) may be examined through a serial port while the CPU (21) is executing instructions normally.

11 Claims, 2 Drawing figures

☐ 24. Document ID: US 5463760 A

L2: Entry 24 of 32 File: USPT Oct 31, 1995

US-PAT-NO: 5463760
DOCUMENT-IDENTIFIER: US 5463760 A

TITLE: Break function in-circuit emulator for a microprocessor with a cache memory

DATE-ISSUED: October 31, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hamauchi; Tetsuji	Tokyo			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
NEC Corporation	Tokyo			JP	03

APPL-NO: 07/ 756199 [PALM]
DATE FILED: September 9, 1991

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	2-237417	September 7, 1990

INT-CL: [06] G06 F 11/00

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US-CL-ISSUED: 395/500; 375/800, 375/375, 375/183.04, 364/232.8, 364/266, 364/DIG.1
US-CL-CURRENT: 703/28; 711/3, 712/43, 714/28

FIELD-OF-SEARCH: 395/375, 395/500, 395/700, 395/800, 395/425, 371/16, 371/16.2, 371/2.2, 371/3, 371/15.1, 371/16.1, 371/16.2, 371/16.5, 371/21.6, 371/22.1, 371/22.6, 371/23, 371/67.1, 371/68.3

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4674089	June 1987	Poret et al.	371/25
4811345	March 1989	Johnson	371/16
4924382	May 1990	Shouda	395/700
4998197	March 1991	Kurakazu et al.	395/800
5053949	October 1991	Allison et al.	345/375
5132971	July 1992	Oguma et al.	371/16.2

ART-UNIT: 232

PRIMARY-EXAMINER: Bowler; Alyssa H.

ASSISTANT-EXAMINER: Shah; Alpesh M.

ATTY-AGENT-FIRM: Whitham, Curtis, Whitham & McGinn

ABSTRACT:

An in-circuit emulator comprising a microprocessor having an input terminal for selecting whether or not the data obtained by accessing an external address should be registered in the cache memory, a register for storing an address for discontinuing the execution of the microprocessor, and a comparator for comparing an address outputted from the microprocessor with the address stored in the register. When the result of comparison is indicative of coincidence, the comparator outputs a coincidence output signal to the above mentioned terminal of the microprocessor, so that the data is inhibited from being registered into the cache memory. Therefore, an external access is performed for the address discontinuing the execution, and accordingly, a break address can be detected by a device external to the microprocessor.

5 Claims, 10 Drawing figures

☐ 25. Document ID: US 5375228 A

L2: Entry 25 of 32 File: USPT Dec 20, 1994

US-PAT-NO: 5375228
DOCUMENT-IDENTIFIER: US 5375228 A

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TITLE: Real-time signal analysis apparatus and method for digital signal processor emulation

DATE-ISSUED: December 20, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Leary; Kevin W.	Walpole	MA		
Rivin; Russell L.	Norwood	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Analog Devices, Inc.	Norwood	MA			02

APPL-NO: 07/ 651743 [PALM]
DATE FILED: February 4, 1991

INT-CL: [05] G06F 11/00

US-CL-ISSUED: 395/575
US-CL-CURRENT: 714/33

FIELD-OF-SEARCH: 371/19, 371/22.1, 371/23, 371/68.1, 371/24, 371/67.1, 395/575

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4674089	June 1987	Poret	371/25
4796258	January 1989	Boyce	371/16
4821269	April 1989	Jackson et al.	371/29.1 X
4843608	June 1989	Fu et al.	371/68.1
4943969	July 1990	Criswell	371/68.1
5043990	August 1991	Doi et al.	371/68.1
5228039	July 1993	Knoke	371/19

OTHER PUBLICATIONS

Signal Analyzers, Model 3560A, Hewlett Packard Company Catalog, 1989, pp. 153-156.
PM 2260 Oscilloscope Signal Processing Software, Philips Prochure, 1989.
A500 Analog VLSI Test System, Teradyne, 1987.
Microprocessor System Development-MIME 600, Pentica Systems, Inc. Brochure, 1989.

ART-UNIT: 233

PRIMARY-EXAMINER: Beausoliel, Jr.; Robert W.

ASSISTANT-EXAMINER: Snyder; Glenn

ATTY-AGENT-FIRM: Koppel & Jacobs

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ABSTRACT:

An emulation system used to debug software for a digital signal processor (DSP) includes a built-in digital signal analyzer which operates upon the same digital signals as those presented directly to and outputted by the DSP, bypassing the signal converters used to convert an input analog signal to digital format and the output digital signal to analog format. A host computer communicates with the digital signal analyzer via firmware in a control processor and personality board, or is alternately connected directly with the analyzer. Communications between the digital signal analyzer and the DSP are through the same contact probe as that used for the emulation software. The analyzer may be used to trigger a software function within the emulator based upon the real-time signal from the DSP, and is also capable of interpolating between successive digital values of an analyzed signal for display purposes.

8 Claims, 7 Drawing figures

☐ 26. Document ID: US 5371551 A

L2: Entry 26 of 32 File: USPT Dec 6, 1994

US-PAT-NO: 5371551
DOCUMENT-IDENTIFIER: US 5371551 A

TITLE: Time delayed digital video system using concurrent recording and playback

DATE-ISSUED: December 6, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Logan; James	Windham	NH	03087	
Goessling; Daniel	Wayland	MA	01778	

APPL-NO: 07/ 968439 [PALM]
DATE FILED: October 29, 1992

INT-CL: [05] H04N 5/14

US-CL-ISSUED: 348/571; 348/714, 358/335, 360/10.1, 369/60
US-CL-CURRENT: 348/571; 348/714, 386/112

FIELD-OF-SEARCH: 360/10.1, 360/33.1, 369/60, 358/188, 358/903, 358/908, 358/194.1, 358/160, 358/183, 358/335, 358/133, 358/22, 348/1, 348/5, 348/7, 348/10, 348/559, 348/560, 348/725, 348/571, 348/722, 348/714

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4862269	August 1989	Sonada et al.	358/160

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4949187	August 1990	Cohen	360/33.1
4963995	October 1990	Lang	358/133
4965662	October 1990	Shiota	358/160
5099319	March 1992	Esch et al.	348/722
5103467	April 1992	Bedlek et al.	369/60
5130792	July 1992	Tindell et al.	348/7
5132992	July 1992	Yurt et al.	348/5
5181114	January 1993	Richards et al.	358/160
5191431	March 1993	Hasegawa et al.	358/335
5283639	January 1994	Esch et al.	348/722

ART-UNIT: 262

PRIMARY-EXAMINER: Powell; Mark R.

ASSISTANT-EXAMINER: Miller; John W.

ATTY-AGENT-FIRM: Allegretti & Witcoff, Ltd.

ABSTRACT:

A broadcast recording and playback device employing a "circular buffer" which constantly records one or more incoming audio or video program signals and a microprocessor for accessing the memory to read a playback signal from the circular buffer to display programming material delayed from its receipt by a selectable delay interval. The circular buffer is implemented by a digital memory. Subsystem comprising the combination of a semiconductor RAM memory and a disk memory operated under the control of a microprocessor such that incoming signals are constantly recorded as received while, at the same time, delayed signals are being read from the memory subsystem at a different memory location selected by a microprocessor to provide a user-selected time delay. A plurality of input signal processors provides one or more programming signals to the memory subsystem in compressed digital form and a separate output signal processor converts the compressed digital information read from the memory into a form suitable for display. The audio/video buffer system operates under the control of a microprocessor which accepts commands from a remote command device or a connected host computer.

8 Claims, 2 Drawing figures

☐ 27. Document ID: US 5355369 A

L2: Entry 27 of 32 File: USPT Oct 11, 1994

US-PAT-NO: 5355369
DOCUMENT-IDENTIFIER: US 5355369 A

TITLE: High-speed integrated circuit testing with JTAG

DATE-ISSUED: October 11, 1994

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INVENTOR-INFORMATION:

NAME	CITY	STATE ZIP CODE	COUNTRY
Greenberger; Alan J.	South Whitehall Township, Lehigh County	PA	
Sam; Homayoon	Wescosville	PA	

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
AT&T Bell Laboratories	Murray Hill	NJ			02

APPL-NO: 07/ 692337 [PALM]
DATE FILED: April 26, 1991

INT-CL: [05] H04B 17/00

US-CL-ISSUED: 371/22.3; 371/22.1
US-CL-CURRENT: 714/727; 714/724, 714/731

FIELD-OF-SEARCH: 371/22.3, 371/22.2, 371/22.1, 371/15.1, 371/16.1, 371/21, 364/481, 395/575MSFile, 324/73.1, 324/158R

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4455661	June 1984	Qureshi	364/900
4710927	December 1987	Miller	371/15
4811345	March 1989	Johnson	371/16
4945536	July 1990	Hancu	371/22.3
5068783	November 1991	Tanagawa et al.	395/575

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
92303308	September 1992	EP	
2589264	April 1987	FR	
2643992	September 1990	FR	

OTHER PUBLICATIONS

Journal of Electronic Testing: Theory and Applications, "In Introduction to the Boundary Scan Standard; ANSI/IDDD Std. 1149.1" by Maunder et al. Mar., 1991, pp. 27-42.
Electronik, Feb. 2, 1989, Messen und Testen, "Verbesserte Prufbarkeit durch strukturierte ASIC-Designs" by Dr. Wolfgang Wach, pp. 31-36, English Abstract of French Patent 2643992.
Motorola Semiconductor Technical Data, DSP96002, by BR575/D, Technical Summary, "96-Bit General Purpose Floating-Point Digital-Signal Processor (DSP)" Motorola, Inc., 1988.
Texas Instruments TMS320C50 DSP Preview Bulletin, p. 4.

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Texas Instruments TMS 320 Family Development Support Reference Guide Hardware Development Tools--TMS320 Emulator (XDS), pp. 5-17 to 5-32.
The Test Access Port and Boundary Scan Architecture, Colin M. Maunder and Rodham E. Tulloss, IEEE Computer Society Press Tutorial, 1990 IEEE, pp. 33 through 77.
Publication: Digital Signal Processing: Technology and Applications, Title: TMS320C50-The Next Generation 35NS Fixed-Point Digital Signal Processor, Author: C Marven, Texas Instruments Ltd., Journal Date: Oct. 19, 1989, Page No.: 5.1/1-8.

ART-UNIT: 233

PRIMARY-EXAMINER: Beausoliel, Jr.; Robert W.

ASSISTANT-EXAMINER: Chung; Phung My

ATTY-AGENT-FIRM: Fox; James H.

ABSTRACT:

The use of the JTAG port provides for boundary scan testing of integrated circuits, thereby allowing for the testing of IC's after they have been mounted into a circuit board. However, the conventional JTAG scheme is limited as to speed, since both the input and output vectors must be serially shifted in and out of I/O buffers along the chip boundaries. The present invention speeds the testing of high-speed core logic circuitry by transferring the test program to a special test data register, which downloads the program to the logic circuitry under test, and uploads the results. This allows the core logic to perform the test at its normal operating speed, while still retaining compatibility with the JTAG standard for other tests.

23 Claims, 5 Drawing figures

☐ 28. Document ID: US 5329471 A

L2: Entry 28 of 32 File: USPT Jul 12, 1994

US-PAT-NO: 5329471
DOCUMENT-IDENTIFIER: US 5329471 A
**** See image for Certificate of Correction ****

TITLE: Emulation devices, systems and methods utilizing state machines

DATE-ISSUED: July 12, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugar Land	TX		
Daniels; Martin D.	Houston	TX		
Coomes; Joseph A.	Missouri City	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

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APPL-NO: 08/ 084787 [PALM]
DATE FILED: June 29, 1993

PARENT-CASE:

CROSS-REFERENCE TO RELATED APPLICATIONS This application is a continuation of Ser. No. 07/911,250 filed Jul. 7, 1992 and now abandoned, which is a continuation of Ser. No. 07/387,549, filed Jul. 31, 1989 and now abandoned, which is a continuation-in-part of Ser. No. 093,463, filed Sep. 4, 1987, now abandoned, which is a continuation-in-part of Ser. No. 057,078, now U.S. Pat. No. 4,860,290, filed Jun. 2, 1987. The related coassigned patent documents listed below are hereby incorporated herein by reference. CROSS REFERENCE TABLE Docket No. PTO Reference Effective Filing Date TI-12033 Patent No. 4 860 290 06/02/1987 TI-12451 Patent No. 5 109 494 12/31/1987 TI-12543 Patent No. 5 101 498 12/31/1987 TI-14083 Serial No. 08/001 915 05/04/1989 TI-14147 Serial No. 07/918 902 05/04/1989 TI-14079 Serial No. 07/347 605 05/04/1989 TI-14080 Patent No. 5 072 418 05/04/1989 TI-14081 Patent No. 5 142 677 05/04/1989 TI-14082 Patent No. 5 155 812 05/04/1989 TI-14145 Serial No. 07/967 942 05/04/1989 TI-14141 Serial No. 07/846 459 07/31/1989 TI-14142 Serial No. 07/832 661 07/31/1989 TI-14143 Serial No. 07/827 549 07/31/1989 TI-14282 Serial No. 07/949 757 07/31/1989 TI-14308 Serial No. 07/979 396 07/31/1989 TI-12016 Serial No. 08/108 775 09/07/1988 TI-13371 Serial No. 08/087/020 09/07/1988 TI-13363 Patent No. 5 084 874 09/07/1988 TI-12015 Patent No. 4 872 169 03/06/1987 TI-12698 Serial No. 07/440 454* 09/04/1987 TI-14312 Patent No. 5 237 672 07/28/1989 TI-14315 Serial No. 07/387 569* 07/28/1989 TI-14316 Serial No. 07/387 455* 07/28/1989 TI-14320 Serial No. 07/386 850* 07/28/1989 TI-13495 Patent No. 5 233 690 07/28/1989 TI-11398 Patent No. 5 140 687 12/31/1986
* = abandoned

INT-CL: [05] G06F 15/20

US-CL-ISSUED: 364/578; 364/DIG.1, 364/264.3, 364/264.5, 364/267.4, 364/267.7, 371/16.2, 395/500
US-CL-CURRENT: 703/23; 703/13, 714/28, 714/30, 714/727

FIELD-OF-SEARCH: 364/578, 364/579, 364/580, 371/16.1, 371/16.2, 371/22.3, 395/500

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4023142	May 1977	Woessner	36/1
4268902	May 1981	Berglund et al.	364/200
4277827	July 1981	Carlson et al.	364/200
4312066	January 1982	Bantz et al.	371/22.3 X
4314333	February 1982	Shibayama et al.	364/200
4441154	April 1984	McDonough et al.	364/200
4513418	April 1985	Bardell, Jr. et al.	371/25
4519078	May 1985	Komonytsky	371/22.3

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4594711	April 1986	Thatte	371/25
4597080	June 1986	Thatte et al.	371/25
4601034	May 1986	Sridhar	371/25
4615029	September 1986	Hu et al.	370/89
4621363	November 1986	Blum	371/25
4680733	July 1987	Duforestel et al.	364/900
4687988	August 1987	Eichelberger et al.	371/22.3
4698588	October 1987	Hwang et al.	324/73R
4701921	October 1987	Powell et al.	371/25
4710931	December 1987	Bellay et al.	371/25
4710933	December 1987	Powell et al.	371/25
4788683	November 1988	Hester et al.	371/16.1
4801870	January 1989	Eichelberger et al.	371/22.3
4855954	August 1989	Turner et al.	364/716 X
4857835	August 1989	Whetsel, Jr.	324/73R
4872169	October 1989	Whetsel	371/22.3
4879688	November 1989	Turner et al.	364/716 X
4896296	January 1990	Turner et al.	365/189.08
5103450	April 1992	Whetsel	371/22.1

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FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
2195185A	March 1988	GB	

OTHER PUBLICATIONS

Y. Mochida et al., "A High Performance LSI Digital Signal Processor for Communication", IEEE Journal on Selected Areas in Communications, vol. SAC-3, No. 2, pp. 347-356, Mar. 1985.
WE DSP16 Digital Signal Processor Information Manual, pp. 1-5, 1987.
Second-Generation TMS320 User's Guide, Texas Instruments, pp. D-1-E-8, Dec. 1987.
P. Gifford, "Sequent's Symmetry Series: Software Breadboarding Caught 95% of the Design Errors", VLSI Systems Design, pp. 2-6, Jun. 1988.
"Application Development Environment", AT&T Technologies, Inc., 1988, Single page.
"DSP56001: 56-Bit General Purpose Digital Signal Processor, Motorola", pp. 1-20, 1988.
G. Sohie, et al., "A Digital Signal Processor with IEEE Floating-Point Arithmetic", IEEE Micro, pp. 49-67, Dec. 1988.
J. R. Boddie, et al., "A Floating Point DSP with Optimizing C Compiler" IEEE 1988, pp. 2009-2012.
"DSP96001: 96-Bit General-Purpose Floating-Point Digital-Signal Processor (DSP), Motorola", pp. 1-22, 1988.
TMS370 Family Data Manual Texas Instruments, pp. 14-6, and 14-11 through 14-16, Mar. 1988.
First-Generation TMS320 User's Guide, Texas Instruments, pp. E-1-E-8, Apr. 1988.
"Test-Bus Interface Unit", Honeywell HTIU214PG, undated, received Jul. 1989.

ART-UNIT: 234

PRIMARY-EXAMINER: Cosimano; Edward R.

ATTY-AGENT-FIRM: Hollander; James F. Donaldson; Richard Kesterson; James C.

ABSTRACT:

An emulation device including a serial scan testability interface having at least first and second scan paths, and state machine circuitry connected and responsive to said second scan path generally operable for emulation control of logical circuitry associated with said emulation device.

69 Claims, 47 Drawing figures

☐ 29. Document ID: US 5325368 A

L2: Entry 29 of 32 File: USPT Jun 28, 1994

US-PAT-NO: 5325368
DOCUMENT-IDENTIFIER: US 5325368 A

TITLE: JTAG component description via nonvolatile memory

DATE-ISSUED: June 28, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
James; Larry C.	West Columbia	SC		
Taylor; Mark A.	Columbia	SC		
Harrison; Chris A.	Lexington	SC		
Simpson; David L.	West Columbia	SC		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
NCR Corporation	Dayton	OH			02

APPL-NO: 07/ 799512 [PALM]
DATE FILED: November 27, 1991

INT-CL: [05] G01R 31/28

US-CL-ISSUED: 371/22.3; 395/575
US-CL-CURRENT: 714/727; 714/30, 714/40, 714/42

FIELD-OF-SEARCH: 371/22.1, 371/22.3, 395/575, 324/158R

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4225957	September 1980	Doty, Jr. et al.	371/15

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4597080	June 1986	Thatte et al.	371/25
4621363	November 1986	Blum	371/25
4635261	January 1987	Anderson et al.	371/25
4701921	October 1987	Powell et al.	371/25
4710931	December 1987	Bellay et al.	371/25
4853929	August 1989	Azuma et al.	371/25
4860290	August 1989	Daniels et al.	371/25
4879717	November 1989	Sauerwald et al.	371/22.3
4918379	April 1990	Jongepier	324/73.1
5115191	May 1992	Yoshimoro	371/22.3
5173904	December 1992	Daniels et al.	371/22.3
5222068	June 1993	Burchard	371/22.3
5260950	November 1993	Simpson et al.	371/22.3

OTHER PUBLICATIONS

IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1--1990, May 21, 1990.
The Wall Street Journal, Sep. 19, 1990 Edition, Advertisement, pp. A16-A17.

ART-UNIT: 233

PRIMARY-EXAMINER: Atkinson; Charles E.

ATTY-AGENT-FIRM: Penrod; Jack R.

ABSTRACT:

Nonvolatile memory is provided on each module of a computer system including one or more modules with each module including a plurality of components including JTAG technology. A test bus operable in accordance with the 1149.1 standard is included in the computer system and is arranged to access the nonvolatile memory. Boundary scan information for the components on a module and also additional information, preferably fully describing all JTAG related characteristics and operations, is stored in the nonvolatile memory. A JTAG bus system is then able to access the module memory and obtain all information required to fully implement JTAG operations for the module.

8 Claims, 25 Drawing figures

☐ 30. Document ID: US 5313618 A

L2: Entry 30 of 32 File: USPT May 17, 1994

US-PAT-NO: 5313618
DOCUMENT-IDENTIFIER: US 5313618 A

TITLE: Shared bus in-circuit emulator system and method

DATE-ISSUED: May 17, 1994

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INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pawloski; Martin B.	Scottsdale	AZ		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Metalink Corp.	Chandler	AZ			02

APPL-NO: 07/ 939678 [PALM]
DATE FILED: September 3, 1992

INT-CL: [05] G06F 11/00, G01R 31/28

US-CL-ISSUED: 395/500; 371/16.2, 364/DIG.1, 364/DIG.2
US-CL-CURRENT: 703/28; 714/28, 714/29

FIELD-OF-SEARCH: 371/16.2, 371/16.1, 395/500, 395/800, 364/578

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4569048	March 1986	Sargent	371/16
4674089	June 1987	Poret et al.	395/500
4677586	June 1987	Magar et al.	395/575
4785416	November 1988	Stringer	395/500
4809167	March 1989	Pawloski et al.	295/500
4847805	July 1989	Ishil et al.	371/16.2
4868822	September 1989	Scott et al.	371/16
4901259	February 1990	Watkins	364/578
4939637	June 1990	Pawloski	395/500
4989207	January 1991	Polstra	371/16.2
5048019	September 1991	Albertsen	371/16.2
5056013	October 1991	Yamamoto	371/16.2
5132971	July 1992	Oguma et al.	371/16.2

ART-UNIT: 235

PRIMARY-EXAMINER: Harrell; Robert B.

ASSISTANT-EXAMINER: Philipp; Timothy L.

ATTY-AGENT-FIRM: Werner; Raymond J.

ABSTRACT:

An in-circuit emulator, alternatively referred to as a microcontroller debugging system, has a control processor having I/O ports and a multiplexed address/data bus port, an emulation processor having I/O ports and a multiplexed address/data bus port, an emulation memory having address inputs, a data bus interface and a

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plurality of two-to-one multiplexers. The in-circuit emulator is configured such that the control processor and the emulation processor each have at least one port directly coupled to the data bus of the emulation memory without the use of external tri-state buffers, this is referred to as the shared bus. An address latch, shared by both processors, has its inputs coupled to the shared bus. The outputs of the address latch form a portion of the emulation memory address input, and are coupled to a corresponding portion of the emulation memory address inputs. The emulation processor is supplied with a clock which is selected from the group consisting of: the same clock input signal used by the control processor, a clock synchronized with the internal clock of the control processor and a clock which is asynchronous with respect to the internal clock of the control processor.

31 Claims, 31 Drawing figures

Terms	Documents
(5142673| 5210862| 5313618| 5325368| 5329471| 5355369| 5371551| 5375228| 5463760| 5488688| 5513338| 5530804| 5535412| 5539901| 5544311| 5546566| 5560036| 5561761| 5566303| 5590354| 5610826| 5621651| 5623673| 5631910| 5640542| 5671172| 5729678| 5812830| 5908392| 5960457| 5999163| 6026503)![pn]	32

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Search Results - Record(s) 31 through 32 of 32 returned.

☐ 31. Document ID: US 5210862 A

L2: Entry 31 of 32 File: USPT May 11, 1993

US-PAT-NO: 5210862
DOCUMENT-IDENTIFIER: US 5210862 A

TITLE: Bus monitor with selective capture of independently occuring events from multiple sources

DATE-ISSUED: May 11, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
DeAngelis; Douglas J.	Woburn	MA		
Maddox; Henry W. J.	Franklin	MA		
Peters; Arthur	Sudbury	MA		
Rathbun; Donald J.	Methuen	MA		
Saltmarsh; William L.	Brockton	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Bull HN Information Systems Inc.	Billerica	MA			02

APPL-NO: 07/ 455667 [PALM]
DATE FILED: December 22, 1989

INT-CL: [05] G06F 11/34

US-CL-ISSUED: 395/575; 364/267, 364/267.2, 364/DIG.1
US-CL-CURRENT: 714/45

FIELD-OF-SEARCH: 364/200, 364/900, 371/15.1, 371/16.1, 371/19

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
3831149	August 1974	Job	371/29.1 X
4100532	July 1978	Farnbach	340/146.2 X

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4166290	August 1979	Furtman	364/900 X
4455624	June 1984	Haag	364/900
4495599	January 1985	Haag	364/900
4651298	March 1987	Currier	364/900
4821178	April 1989	Levin	364/200
4845615	July 1989	Blasciak	364/200
4937740	June 1990	Agarwal	371/19 X

ART-UNIT: 236

PRIMARY-EXAMINER: Beausoliel; Robert W.

ATTY-AGENT-FIRM: Clapp; Gary D. Solakian; John S.

ABSTRACT:

A monitor device for selectively detecting and recording conditions at selected points within a system during operation, including a trigger enable memory for storing selectable trigger enabling codes wherein each code corresponds to a trigger signal representing the occurrence of a corresponding condition to be detected, a trigger generation device connected from first selected points and responsive to selected conditions thereupon for generating the trigger signals representing the occurrence of selected conditions, a trigger output device responsive to the enabling codes and the trigger signals for providing trigger outputs upon the occurrence of a trigger signal corresponding to a selected trigger enabling code, and a silo bank memory connected from second selected points and responsive to the trigger outputs for recording conditions present at the second points.

30 Claims, 5 Drawing figures

☐ 32. Document ID: US 5142673 A

L2: Entry 32 of 32 File: USPT Aug 25, 1992

US-PAT-NO: 5142673
DOCUMENT-IDENTIFIER: US 5142673 A

TITLE: Bus monitor with dual port memory for storing selectable trigger patterns

DATE-ISSUED: August 25, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
De Angelis; Douglas J.	Woburn	MA		
Maddox; Henry W. J.	Franklin	MA		
Peters; Arthur	Sudbury	MA		
Rathbun; Donald J.	Methuen	MA		
Saltmarsh; William L.	Brockton	MA		

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ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Bull HN Information Systems Inc.	Billerica	MA			02

APPL-NO: 07/ 455664 [PALM]
DATE FILED: December 22, 1989

INT-CL: [05] G06F 11/34

US-CL-ISSUED: 395/575; 364/267, 364/267.2
US-CL-CURRENT: 714/39

FIELD-OF-SEARCH: 371/19, 371/15.1, 371/16.1, 364/2MSFile, 364/9MSFile

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
3707725	December 1972	Dellheim	371/19
4100532	July 1978	Farnback	340/146.3MA
4445192	April 1984	Haag et al.	364/900
4651298	March 1987	Currier, Jr.	364/900
4845615	July 1989	Blasciak	364/200
4937740	July 1990	Agawal et al.	371/19
5001714	March 1991	Stark et al.	371/26

ART-UNIT: 236

PRIMARY-EXAMINER: Smith; Jerry

ASSISTANT-EXAMINER: Mychung; Phung

ATTY-AGENT-FIRM: Clapp; Gary D. Solakian; John S.

ABSTRACT:

A monitor for selectively detecting and recording conditions at selected points within a system includes a trigger memory for storing patterns of trigger signals, wherein each pattern of trigger signals corresponds to a selected condition to be detected on first points of the system. The trigger memory includes a first port having a read address input connected from the first points and a data output connected to trigger output logic for providing patterns of trigger signals corresponding to the conditions to be detected. Each pattern of trigger signals is stored in the trigger memory location whose address corresponds to a pattern of signals from the first points representing the corresponding condition to be detected. The trigger memory is a dual port memory having a second port with a write address input and a data input for receiving trigger patterns to be stored therein. The method for generating the trigger patterns includes generating a first trigger pattern map and, from the first map, a second trigger pattern map to be written into a trigger memory which includes a plurality of submemories, wherein each submemory stores a portion of the trigger patterns.

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L9: Entry 4 of 4 File: USPT Nov 5, 1996

DOCUMENT-IDENTIFIER: US 5572689 A

**** See image for Certificate of Correction ****

TITLE: Data processing system and method thereof

Detailed Description Paragraph Table (2):

3.3.3 Direct and Inverted Access to the CMA 3.3.4 Allocating CMA Space Example #1: CMA used for Data Storage Only Example #2: Instruction Cache, PC and CMA pages Example #3: CMA used for Program and Data Example #4: Program Shifted Example #5: Adding a Jump Table to Example #4 Example #6: Adding a CMA Stack to Example #4 Example #7: Adding Vector and Scalar Storage to Example #4 Example #8: Bringing all the pieces together 3.4 Association Engine Initialization 3.5 Post Operation 3.5.1 Host Transfer Modes Random Access Mode Host Stream Access Mode 3.5.2 Association Engine Transfer Modes Input Indexing Examples using the ILMR Input Tagging 3.5.3 Host Memory Map for the Association Engine 3.6 Association Engine Operation 3.6.1 Association Engine Macro View 3.6.2 Detailed Description of Host and Association Engine interactions Input Valid Bits Fill Then Compute Compute While Filling Association Engine Interaction With The Association Engine' 3.6.3 Association Engine Micro View of Instruction Flow 3.6.4 Association Engine Exception Model Reset Exception Scalar Exceptions Vector Exceptions Port Error Exceptions Interpreting Multiple Port Error Exceptions 3.6.5 Microcode Program Structure Initialization and Looping Multiple Loops Semaphore passing between two Association Engines Conditional Execution 3.7 Microcode Initiated Port Write Operations 3.8 Association Engine Bus Configurations 3.8.1 Association Engine Port Switches and Taps 3.8.2 Bus Port Collisions and Errors Association Engine Collision Condition Association Engine Contention Condition Association Engine Interleave Association Engine Switch Contention 3.8.3 Association Engine Ring Configuration 3.8.4 Two Dimensional Association Engine Configuration SECTION 4 Association Engine Bus Operation 4.1 Association Engine Port Timing 4.1.1 Host Random Accesses 4.1.2 Host Random Address Transfer West to East 4.1.3 Host Random Address and Data Transfer North and South 4.1.4 Host Random Address/Data Transfer North/South with Early Termination 4.1.5 Host Stream Read 4.1.6 Host Stream Write Accesses 4.2 Association Engine Master Operations 4.2.1 Association Engine Write Operation All Valid Data 4.2.2 Association Engine Write Operation Partial Valid Data 4.2.3 Association Engine write Collision Timing 4.3 Miscellaneous Timing 4.3.1 Association Engine BUSY Output Timing 4.3.2 Association Engine write Timing with Run/Stop Intervention 4.3.3 Interrupt Timing 4.3.4 Reset Timing 4.3.5 IEEE 1149.1 Test Access Port (TAP) Timing SECTION 5 Overview of Selected Topics 5.1 Saturation Protection 5.2 Communications Between Data Processors: Switch and Tap 5.3 Multi-Port Data Processor 5.4 Extended Length Operations in a Data Processor 5.5 Data movement Operations in a Data Processor 5.5.1 Instructions "dadd", "daddp", "dmin", "dminp", "dmax", and "dmaxp" 5.5.2 Instruction "dsrot" 5.6 Multi-Level Conditional Execution of Instructions 5.6.1 Instructions "vif", "velse", and "vendif" 5.6.2 Instructions "dskip" and "dskipe " 5.6.3 Instructions "repeat" and "repeate" 5.7 Data Processor Architecture 5.8 Loading Incoming Data into a Data Processor 5.9 Stalling Technique and Mechanism for a Data Processor 5.10 Maximum and Minimum Determinations 5.10.1 Instructions "colmax", "rowmax", "locmax", "colmin", "rowmin", and "locmin" 5.10.2 Instructions "vmaxp", "vmax", "vminp", and "vmin ", "maxp", "max", "minp", and "min" 5.11 Inverted Access to the Coefficient Memory Array (CMA) 14

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L9: Entry 4 of 4 File: USPT Nov 5, 1996

US-PAT-NO: 5572689
DOCUMENT-IDENTIFIER: US 5572689 A
** See image for Certificate of Correction **

TITLE: Data processing system and method thereof

DATE-ISSUED: November 5, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gallup; Michael G.	Austin	TX		
Goke; L. Rodney	Austin	TX		
Seaton, Jr.; Robert W.	Austin	TX		
Lawell; Terry G.	Austin	TX		
Osborn; Stephen G.	Austin	TX		
Tomazin; Thomas J.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Motorola, Inc.	Schaumburg	IL			02

APPL-NO: 08/ 408045 [PALM]
DATE FILED: March 21, 1995

PARENT-CASE:
This is a divisional of application Ser. No. 08,040,779, filed Mar. 31, 1993, now abandoned.

INT-CL: [06] G06 F 9/315

US-CL-ISSUED: 395/376; 364/DIG.2
US-CL-CURRENT: 712/200

FIELD-OF-SEARCH: 395/375

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
3287703	November 1966	Slotnick	340/172.5

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☐	3796992	March 1974	Nakamura et al.	340/147LP
☐	4463445	July 1984	Grimes	364/900
☐	4470112	September 1984	Dimmick	364/200
☐	4488218	December 1984	Grimes	364/200
☐	4546428	October 1985	Morton	364/200
☐	4809169	February 1989	Sfarti et al.	364/200
☐	5067095	November 1991	Peterson et al.	395/24
☐	5073867	December 1991	Murphy et al.	395/27
☐	5083285	January 1992	Shima et al.	395/24
☐	5086405	February 1992	Chung et al.	364/748
☐	5140523	August 1992	Frankel et al.	364/420
☐	5140530	August 1992	Guha et al.	395/13
☐	5140670	August 1992	Chua et al.	395/24
☐	5146420	September 1992	Vassiliadis et al.	364/757
☐	5148515	September 1992	Vassiliadis et al.	395/27
☐	5150327	September 1992	Matsushima et al.	365/189
☐	5150328	September 1992	Aichelmann, Jr.	365/189
☐	5151874	September 1992	Jeong et al.	364/752
☐	5151971	September 1992	Jousselin et al.	395/27
☐	5152000	September 1992	Hillis	395/800
☐	5155389	October 1992	Furtek	307/465
☐	5155699	October 1992	Chung et al.	364/766
☐	5165009	November 1992	Watanabe et al.	395/27
☐	5165010	November 1992	Masuda et al.	395/27
☐	5167008	November 1992	Engeler	395/27
☐	5168573	December 1992	Fossum et al.	395/800
☐	5175858	December 1992	Hammerstrom	395/800
☐	5182794	January 1993	Gasperi et al.	395/23
☐	5197030	March 1993	Akaogi et al.	365/200
☐	5197130	March 1993	Chen et al.	395/325
☐	5226171	July 1993	Hall et al.	395/800
☐	5230057	July 1993	Shido et al.	395/800

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Document No. 07/600,784 Name Gardner et al. Filing Date Oct. 22, 1990.
Document No. 07/898,189 Name Gardner et al. Filing Date Jun. 12, 1992.
"Neural Networks Primer Part VII" published in AI Expert in May 1989 and written by Maureen Caudill, pp. 51 through 58.

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"Neural Networks Primer Part VIII" published in AI Expert in Aug. 1989 and written by Maureen Caudill, pp. 61 through 67.
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Document No. 07/600,982 Name Gardner Filing Date Oct. 22, 1990.
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ART-UNIT: 235

PRIMARY-EXAMINER: Treat; William M.

ATTY-AGENT-FIRM: Apperley; Elizabeth A.

ABSTRACT:

A data processing system (55) and method thereof includes one or more data processors (10). Data processor (10) is capable of performing both vector operations and scalar operations. Using a single microsequencer (22), data processor (10) is capable of executing both vector instructions and scalar instructions. Data processor (10) also has a memory circuit (14) capable of storing both vector operands and scalar operands.

8 Claims, 319 Drawing figures

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L9: Entry 1 of 4 File: USPT Dec 7, 1999

US-PAT-NO: 6000051
DOCUMENT-IDENTIFIER: US 6000051 A

TITLE: Method and apparatus for high-speed interconnect testing

DATE-ISSUED: December 7, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nadeau-Dostie; Benoit	Aylmer			CA
Cote ; Jean-Francois	Aylmer			CA

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Logic Vision, Inc.	San Jose	CA			02

APPL-NO: 08/ 948842 [PALM]
DATE FILED: October 10, 1997

INT-CL: [06] G01 R 31/28

US-CL-ISSUED: 714/727; 714/731, 327/144
US-CL-CURRENT: 714/727; 327/144, 714/731

FIELD-OF-SEARCH: 714/731, 714/727, 714/726, 714/724, 714/729, 714/733, 714/734, 714/814, 714/815, 714/30, 327/144, 327/141, 377/77, 377/78, 377/81

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4494066	January 1985	Goel et al.	714/726
☐	5109190	April 1992	Sakashita et al.	714/727
☐	5463338	October 1995	Yurash	327/202
☐	5774476	June 1998	Pressly et al.	714/726

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IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Standard 1149.1-1990 (Includes IEEE Standard 1149.1a-1993) pp. 1-1 to 1-5; 5-1 to 5-16.

ART-UNIT: 274

PRIMARY-EXAMINER: Tu; Trinh L.

ATTY-AGENT-FIRM: Skjerven, Morrill, MacPherson, Franklin & Friel LLP Klivans; Norman R.

ABSTRACT:

A method of testing high speed interconnectivity of circuit boards having components operable at a high speed system clock, employing an IEEE 1149.1 standard test method in which test data is shifted into and from the components at the rate of a test clock during Shift.sub.-- In and Shift.sub.-- Out operations, and having an Update operation and a Capture operation between the Shift.sub.-- In and Shift.sub.-- Out operations, the components including a first group of components capable of performing the Update and Capture operations at the rate of the Test Clock only and a second group of components capable of performing the Update and Capture operations at the rate of the system clock, the method comprising the steps of performing the Shift.sub.-- In operation in all of the components concurrently at the rate of the Test Clock; performing the Update and Capture Operations in the first group of components at the rate of the Test Clock; and performing the Update and Capture Operations in the second group of components at the rate of the system Clock. The method employs a novel integrated circuit, test controller and boundary scan cells.

43 Claims, 9 Drawing figures

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L9: Entry 1 of 4 File: USPT Dec 7, 1999

DOCUMENT-IDENTIFIER: US 6000051 A
TITLE: Method and apparatus for high-speed interconnect testing

Detailed Description Text (5):
FIG. 2 illustrates the circuit board 10 in more detail than FIG. 1 in order to better illustrate the boundary scan cell chain 20 and the plurality of boundary scan cells 28 associated with the core of each integrated circuit and the serial interconnection of the cells for serial data transfer. Circuit Board 10 is formed with an edge card connector 30 to connect the board to external equipment, including the automatic test equipment. FIG. 2 shows three integrated circuits 12 and one conventional off-the-shelf IEEE 1149.1 compliant integrated circuit 14. As in FIG. 1, the main components of the two types of integrated circuits have been identified--core logic 18, boundary scan cells 28, Test Access Port 22 and Test Controller 26.

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L13: Entry 1 of 1 File: USPT Jun 30, 1998

US-PAT-NO: 5774476
DOCUMENT-IDENTIFIER: US 5774476 A

TITLE: Timing apparatus and timing method for wrapper cell speed path testing of embedded cores within an integrated circuit

DATE-ISSUED: June 30, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pressly; Matthew D.	Austin	TX		
Giles; Grady L.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Motorola, Inc.	Schaumburg	IL			02

APPL-NO: 08/ 794743 [PALM]
DATE FILED: February 3, 1997

INT-CL: [06] G06 F 11/00

US-CL-ISSUED: 371/22.31
US-CL-CURRENT: 714/726

FIELD-OF-SEARCH: 371/22.31, 371/22.5, 371/22.1, 324/73.1, 395/183.06

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5054024	October 1991	Whetsel	371/22.3
☐	5220281	June 1993	Matsuki	324/158
☐	5229657	July 1993	Rackley	307/443
☐	5260947	November 1993	Posse	371/22.3
☐	5260949	November 1993	Hashizume et al.	371/22.3
☐	5260950	November 1993	Simpson et al.	371/22.3

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ART-UNIT: 275

PRIMARY-EXAMINER: Canney; Vincent P.

ATTY-AGENT-FIRM: Witek; Keith E.

ABSTRACT:

Wrapper cells (16 and 18) are coupled to inputs and outputs of an embedded core (14) within an integrated circuit (10). The wrapper cells (16 and 18) are used to test timing specifications of the embedded core after the embedded core has been integrated on-chip with other peripheral logic (12). In order to accurately measure the timing specifications, test circuits (FIGS. 6-8) are formed on chip with the wrapper where the test circuits are used to measure clock skew a like internal integrated circuit (IC) parameters. The clock skew and other measured internal IC parameters are used to accurately test the timing specification of the embedded core with reduced uncertainty.

38 Claims, 8 Drawing figures

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L13: Entry 1 of 1 File: USPT Jun 30, 1998

DOCUMENT-IDENTIFIER: US 5774476 A
TITLE: Timing apparatus and timing method for wrapper cell speed path testing of embedded cores within an integrated circuit

Brief Summary Text (9):
A second prior art method is to use IEEE 1149.1 (JTAG) boundary-scan cells on all core ports. This method allows use of the 1149.1 Test Access Port (TAP) to serially shift data into and out of these boundary-scan cells for controllability of core inputs and observability of core outputs, respectively, through use of the IEEE 1149.1 instructions such as INTEST. This prior art method has never addressed the issue of testing timing specifications for embedded core input and outputs, and therefore, applies vectors with sufficiently large time intervals between launch and capture events that failure to meet timing specifications alone will not cause a production test failure.